MINIATURE DIGITAL TELEMETRY SYSTEM EMPLOYING CYCLIC TIME MULTIPLEXING DESIGNED FOR POTENTIOMETRIC TRANSDUCERS

William Gadino

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

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by

William Gadino

Thesis Advisors: G. D. Ewing
R. Panholzer

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Miniature Digital Telemetry System Employing Cyclic Time Multiplexing Designed for Potentiometric Transducers

by

William Gadino
Lieutenant, United States Navy
B.E.E., Villanova University, 1968

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ABSTRACT

This paper describes the design and testing of a miniature multi-channel digital telemetry system designed specifically for use in remote controlled model aircraft experiments coordinated by the Aeronautical Engineering Department at the Naval Postgraduate School. The avionics package comprised of data encoder/multiplexer circuitry and a transmitter is lightweight, inexpensive, small in physical size, has low current drain and is capable of transmitting up to nine channels of data. The system was designed specifically for transducers with potentiometric outputs although transducers having voltage or current outputs can be interfaced with the system.

The thesis emphasizes the engineering design requirements and working design models to achieve efficient system performance.

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TABLE OF ABBREVIATIONS

BCD	Binary Coded Decimal
Tc	Cycle Time
Vdc	Direct Current Voltage
FDM	Frequency Division Multiplex
IC	Integrated Circuit
kΩ	1000 ohms
max	Maximum
µF	Micro-farad
µsec	Micro-second
mA	Milliamperes
ms	Milliseconds
MUX	Multiplexer
ns	Nanoseconds
NiCad	Nickel Cadmium
Op Amp	Operational Amplifier
pc	Printed circuit
pF	Pico-farad
RF	Radio Frequency
RPV	Remotely Piloted Vehicle
sync	Synchronization
TDM	Time Division Multiplex
TTL	Transistor-transistor-logic
typ	Typical

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I would like to express my sincere gratitude to the following people who helped in the completion of this project. First, Dr. Gerald D. Ewing, Professor of Electrical Engineering, who was a constant source of knowledge and encouragement. Dr. Rudolf Panholzer, who aided in the digital IC designs. LT Laird W. Stanton, USN, who provided many useful hints in both the encoder and decoder designs. Dr. Howard Power, Professor of Aeronautical Engineering provided most of the early direction in system approach and transducer requirements. Mr. Paul Sparks aided in adapting the commercial transmitter and receiver units to both electronic specifications and packaging requirements. My wife, Aleta, who typed the first manuscript.

I. INTRODUCTION

This paper describes the design and subsequent testing of a miniature multi-channel telemetry system for use in RPV research at the Naval Postgraduate School.

A. AIRCRAFT CONSIDERATIONS

For many years it has been recognized that a scale model RPV could be a valuable research tool for investigating aircraft flight characteristics. The expenses involved in changing the flying qualities of full scale aircraft after the design has been "frozen" preclude any major redesigns. RPV's, on the other hand, can provide the designers with an excellent, low cost instrument allowing important dynamic aircraft parameters to be varied to achieve design optimization.

In the past, wind tunnel data and theory have been relied upon to predict performance and handling characteristics during the design process. Unfortunately the wind tunnel permits static measurements only. As a consequence, required dynamic results are missing. The validity of wind tunnel data is also suspect due to the close proximity of the tunnel walls to the model and the resulting changes in the air flow field.

With a scale model the above problems are solved and the RPV also permits the engineer to study dangerous flight regimes, such as those required to research spin and stall

characteristics, without endangering full-scale aircraft or human life.

Before the RPV can be effectively utilized for the above cited design efforts, a simple, accurate and inexpensive system for relaying air-to-ground flight data must be available. This telemetering system must also be compatible with the limited space and weight requirements of a scale RPV. These last restrictions prohibit the installation of a data recording system for analyzing information after each flight because there would be a need for encoding and multiplexing (or multi-channel data recorder) circuitry in addition to the recorder, not to mention that all the data is subject to loss in the event of a crash. A telemetry system would be free of these difficulties and it also provides the testing engineer with real-time data on the RPV performance.

The telemetry system used is, to a certain extent, dependent upon the transducers required to measure the important flight characteristics. Table I shows a typical set of flight parameters required to determine aircraft real-time motion. Research efforts disclose that all of these parameters could be measured with commercially available transducers (or transducers fabricated at NPS) having potentiometric outputs. It was desirable to have this type of sensor because low power is normally required for operation.

PARAMETERS
a) angle of attack
b) slip angle
c) yaw angle
d) altitude
e) air speed
f)
g) acceleration in three planes
h)

Table I. Parameters in a Typical RPV

B. TELEMETRY SYSTEM CONSIDERATIONS

The general system layout includes three major areas as depicted in figure 1. The avionics package includes sensors, encoding and multiplexing circuitry to put the data signals in a form suitable for transmission, a transmitter and a rechargeable NiCad battery for power.

The ground based equipment will include a receiver, a decoder/demultiplexer to allow separation of the multiplexer data stream and readout devices which may include meters, data recorders, chart recorders, digital displays or the like. It should be noted that the aircraft will also contain an electronics package to permit remote piloting from the ground.

It was felt that the major design problems to be encountered were in the avionic package because of size constraints, power consumption and sensor interfacing. The size was dictated by the aircraft to be used.

It was desired to house the avionics package in a space four inches long, two inches wide, and three inches high. The weight limitation was 1/2 pound including batteries. Suitable flying time can still be achieved with commercial

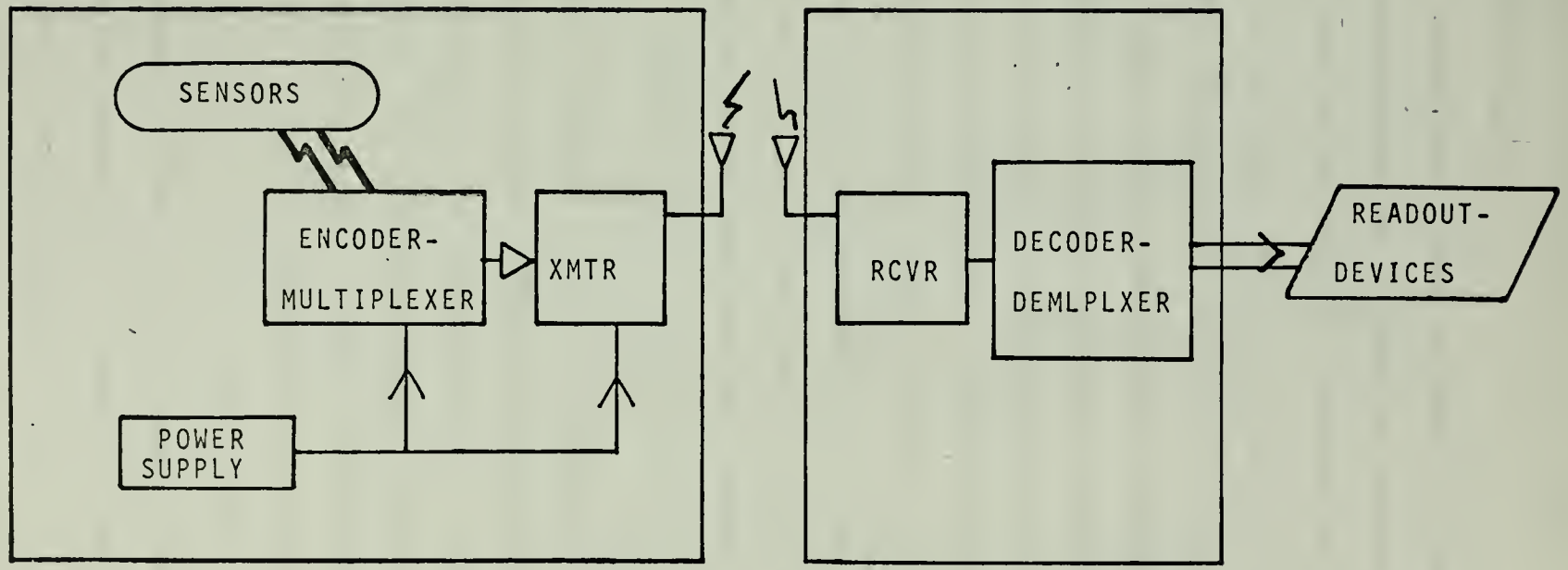


Figure 1. Block Diagram of Typical Telemetry System

light-weight NiCads if the total supply current is limited to 250 mA or less.

Most transducers used in modern telemetry systems have either potentiometric, voltage or current outputs. These outputs must be periodically sampled by some method that will encode and multiplex the data both accurately and reliably. The method must have the ability to transmit multiple data channels representing the various sensor outputs. There are no bandwidth limitation problems foreseen because the movements of an aircraft do not change very rapidly relative to electronic response times. This fact permits the transducers to be sensed at relatively low data rates. Frequency variations for flight characteristics are usually not above one hertz. As will be pointed out in later chapters, the telemetry sampling rates employed are around 50 hertz; hence, the Nyquist sampling criteria was amply satisfied.

C. SURVEY OF METHODS FOR DATA TRANSMISSION

There are several techniques available with signal formation suitable for this application. Some of the more widely used methods for telemetry encoding are shown in figure 2. The classical methods of FDM and TDM were available for multiplexing. Prior to choosing any one method, it was decided to investigate the methods used in today's Remote Control (RC) systems for model planes because these systems experience similar constraints. Modern RC equipments are digitally proportional systems employing what is commonly referred to as pulse position modulation. This method may be found in

the more technical literature as "Cyclic Time Multiplexing (CTM) with Signal Sequence Switching."

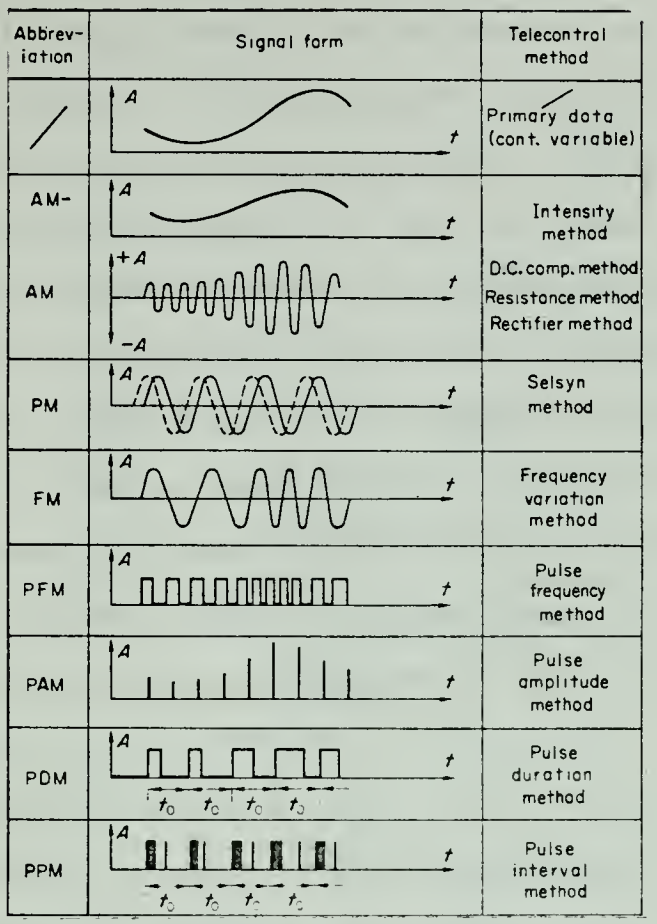


Figure 2. Analog Telemetry Methods

Further investigation indicated that CTM was the best approach because: 1) the telemetry system could interface with existing hardware if needed (e.g. with RC servo units for use as readout devices), 2) the derivation of control or "clock" signals from electronics already in the RPV was possible and 3) information was available on the shortcomings of commercial RC systems used in scale models.

With CTM the data generators (or sensors) are continually interrogated in a constant and repeated sequence. There are various types of CTM with signal sequence switching being a method used to relay data in one direction only, which is all that is required for this system. Figure 3 illustrates this CTM scheme with related waveforms. Referring to figure 3a, observe that the outputs of the individual input devices S1 to S3 are sampled sequentially by the scanner which converts the data present into transmission signals. At the receiving end, these signals are reconstructed by passing out a piece of data at each position of the scanner. Note that these data bits must be stored in locations R1 to R3 for a fixed period of time to ensure proper operation of the output devices O1 to O3. Locations R1 to R3 are refilled with new data at each rotation of the scanner. There must also be a synchronization signal at the beginning (or end) of each rotation to ensure synchronous running of the receiver and transmitter scanners. The cycle time (Tc) is much longer than any of the individual signals. Tc is determined by the reciprocal of the maximum sampling rate desired (e.g. a rate of 50 hertz needs a Tc=1/50=20ms). The lengths of the individual sensor signals is then determined by the total number of data channels required and the length of the sync pulse. Figures 3b and 3c depict two waveform variations that may be employed. In figure 3c the sampling is done at fixed time for each sensor while in 3b the end of sample time for one data generator starts the sample time of the next and so

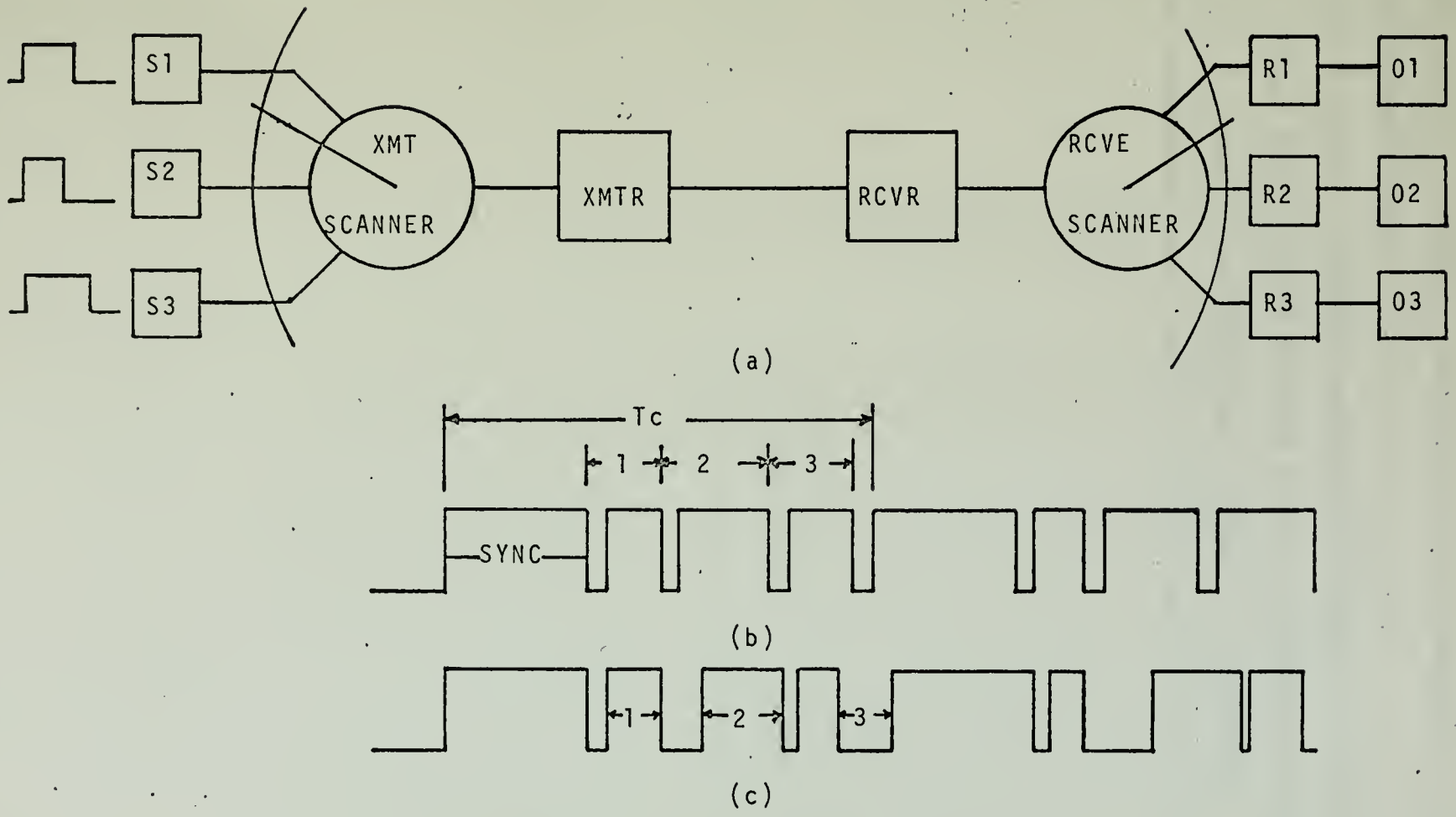


Figure 3. CTM Sampling Schemes: (a) Block Diagram, (b) Variable Frame Rate, (c) Fixed Interval for each Channel.

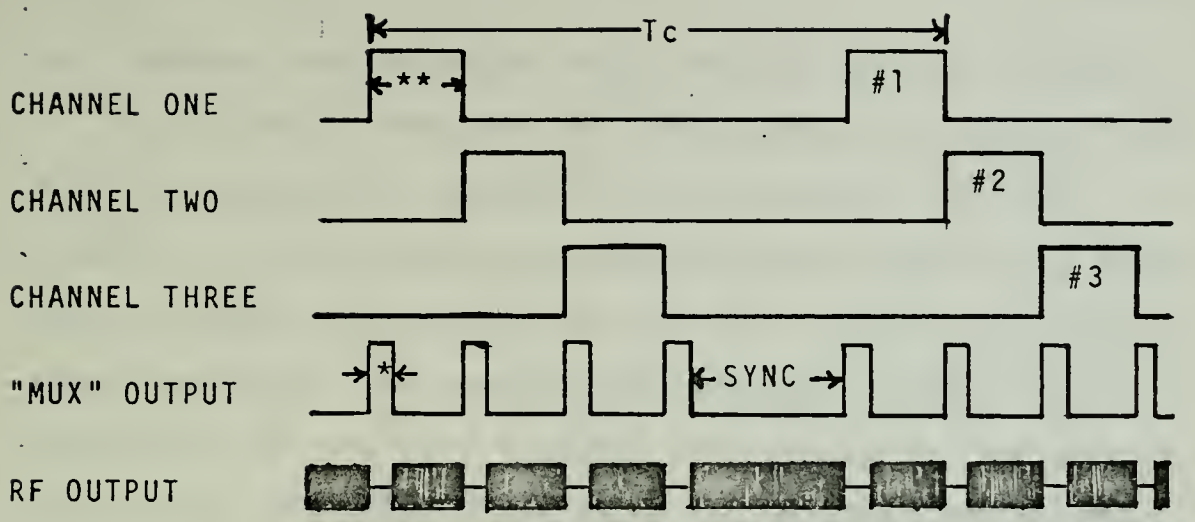
forth (the sync pulse may be placed at the beginning or end of the pulse train).

The following chapters describe the system in more detail with a chapter each devoted to: a) encoder-multiplexer design, b) decoder-demultiplexer design, c) transmitter, receiver considerations, readout devices, and d) system testing.

II. ENCODER-MULTIPLEXER DESIGNS

While the encoder-multiplexer theory was easily specified, the actual implementation with components proved to be a more difficult task. Three different circuits evolved from the efforts to design a workable encoder. Although only one circuit was chosen for the final system package, it is felt that all three designs should be explained because: 1) they all accomplished the desired task, and 2) there were strengths and weaknesses associated with each method which can be of benefit to future designers in this area. All three designs were similar in that integrated circuits (IC's) were used throughout. The first design used digital (TTL) IC's, the second design utilized linear IC's and the third design employed both digital and linear IC's.

All three designs produce outputs of varying pulse widths proportional to respective sensor outputs. Figure 4 illustrates the typical waveforms for a three channel encoder. The individual channel widths vary from one to two milliseconds while the multiplexer (MUX) "on" pulse is 250 μsec. This 250 μsec pulse is then used to key a transmitter. This method of modulation reduces the possibility of the receiver circuits being triggered by interference which would yield erroneous data. Observe that the MUX output waveform of figure 4 is similar to that of figure 3c with the exceptions that 1) the sync pause appears at the end of the pulse train and 2) the signal has been inverted. The question of whether



* 250usec

** 1-to-2ms

Figure 4. Typical Encoder Outputs.

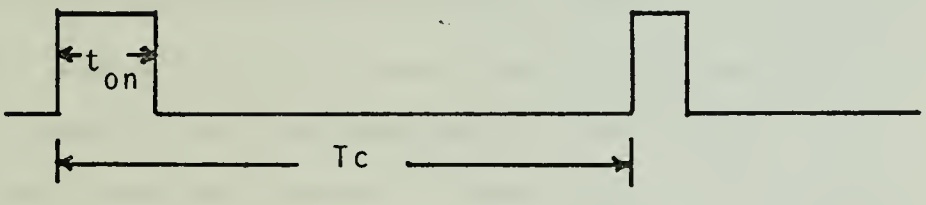


Figure 5. Output of Typical Channel from Aircraft Control Circuitry.

the signal needs to be inverted or not depends on how the transmitter is modulated (to be discussed in a later chapter).

A. ENCODER IMPLEMENTATION USING DIGITAL (TTL) IC APPROACH

This circuit makes use of four different Signetics IC's: a dual retriggerable monostable multivibrator (N74123), an 8-line to 1-line data selector/multiplexer (N74151), a quadruple 2-input positive NOR gate (N7402), and a 4-bit binary counter (N7493). To enhance understanding selected product information on the IC's is given in Appendix A. One each of the N74151, N7402 and N7493 chips are required for any encoder up to eight channels (16 channels if one used a 16-line to 1-line data selector/multiplexer (74150)), while N/2 + 1 multivibrators are required with N being the largest even number of channels desired (e.g. eight channels requires 8/2 + 1 = 5).

The following is a discussion of how eight data channels are generated and time multiplexed. The overall block diagram is given in figure 6. Before proceeding with this circuit, it is important to note that this design is based on the fact that a cycle rate or frame rate already exists in the aircraft control and instrumentation electronics. The waveform output from any channel in the control electronics (i.e. to remotely pilot the aircraft) is pictured in figure 5. Although the "on" time (labeled "t_{on}" in the figure) may vary, there is always a fixed interval (16-20ms depending on the control system used) between rising edge pulses. This allows the use of this signal as a "clock" for the telemetry

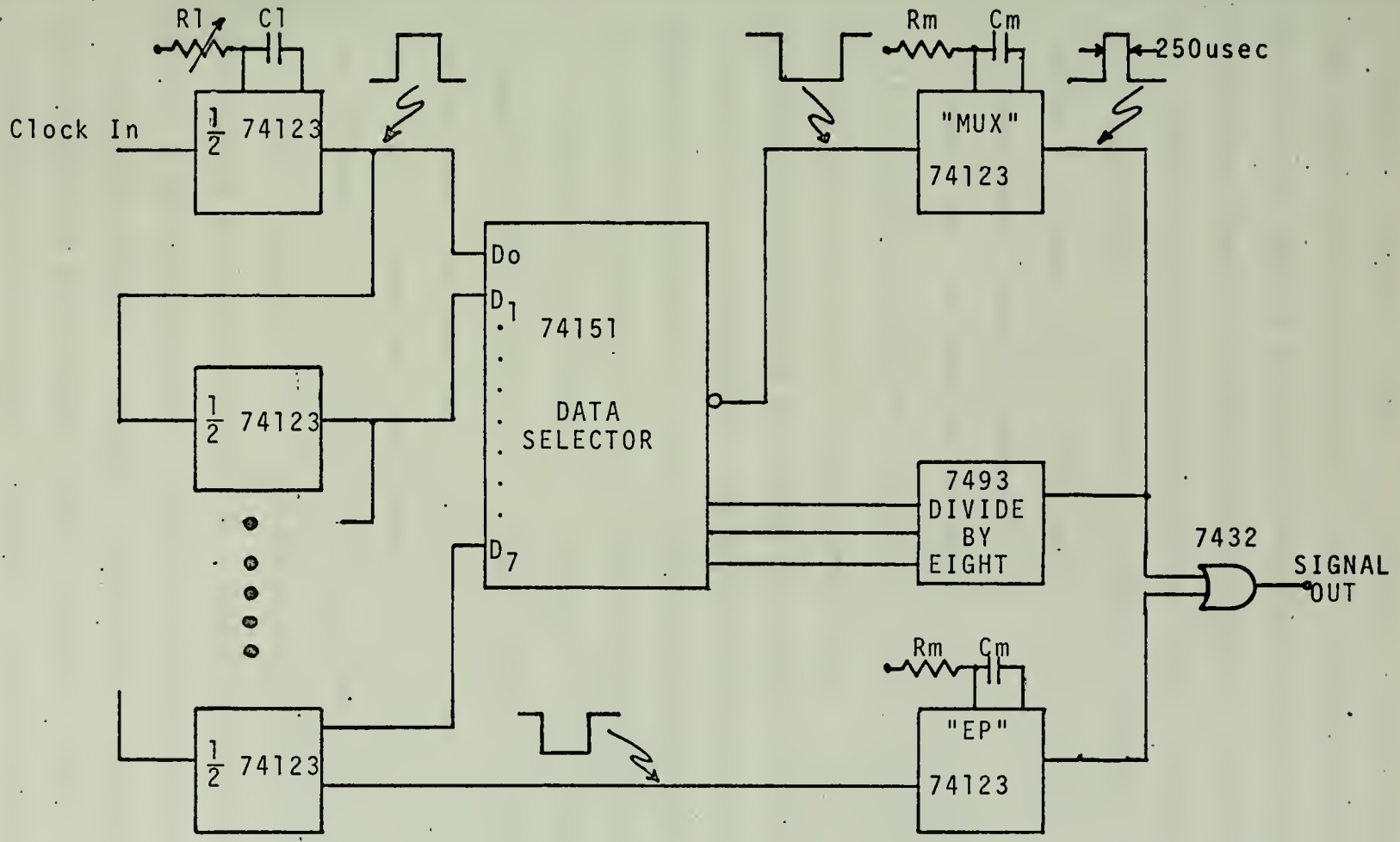


Figure 6. TTL Encoder Block Diagram

encoder. The clock input is applied to the rise trigger of the channel one monostable. The "Q" output immediately goes HIGH for an amount of time determined by R1C1 where R1 is the potentiometric output from a sensor. The "Q" output is then simultaneously applied to data input zero (D_o) of the data multiplexer and the fall triggered input of the channel number two monostable. This sequence is repeated until eight channels have been synthesized.

Note that the complement output "W" is applied to the fall triggered input of another monostable whose quasistable period has been set, by R_mC_m, to 250 μsec. The "Q" output of this monostable is then used to trigger the 7493 counter (the 7493 is triggered on the falling edge of an input pulse), which is configured to give a divide by eight count. These last three components form the time multiplexing desired in the following manner (refer to figure 7 for related waveforms): assume the 7493 contains the binary number "1" (001); then the D1 input on the 74151 will be connected to the "W" output. This allows the complement of D's input to be seen at "W". Since the "W" output is tied to the fall trigger of the 74123 a positive 250 μsec pulse is generated at the "Q" output and applied to the 7493. Since the 7493 is fall triggered, the trailing edge of the 250 μsec pulse increments the 7493 by one count. Now the 7493 contains the binary number two (010) and this causes input D2 of the 74151 to be connected to the "W" output. The "W" output immediately goes HIGH again because channel number two's output is in the

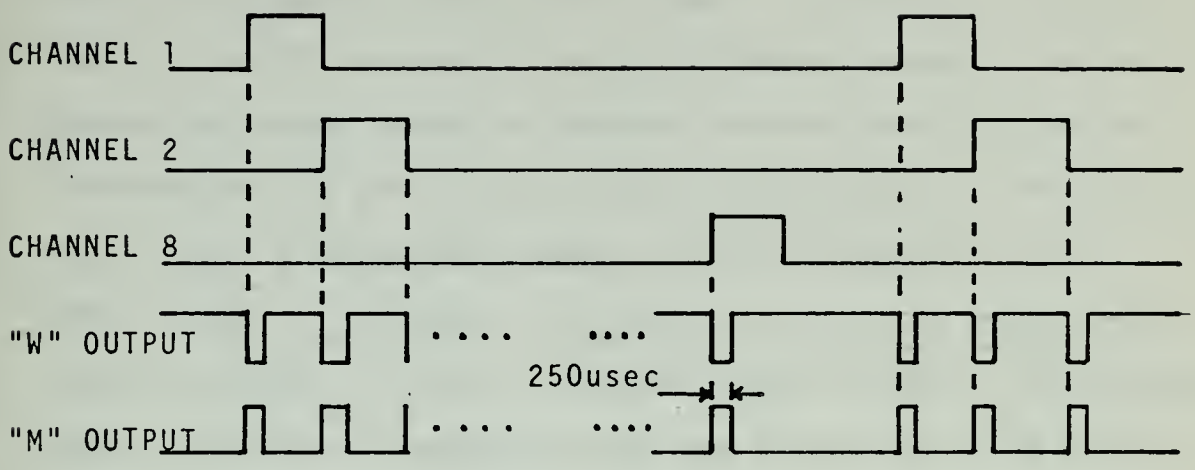


Figure 7. Multiplexer Waveforms.

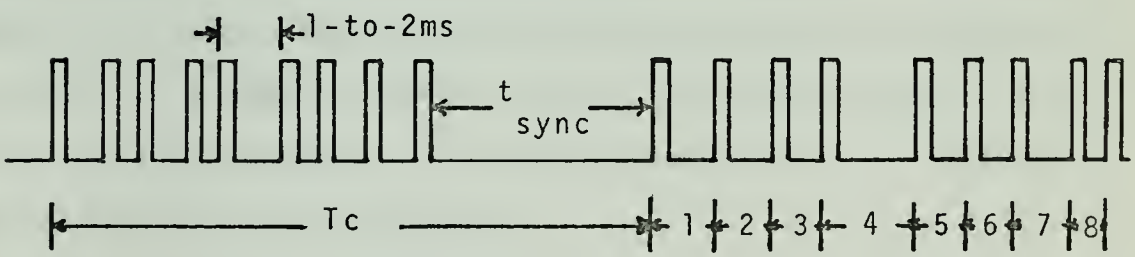


Figure 8. "MUX" Output Waveform.

stable (or LOW) state at this time. After 1-2ms (depending on the sensor position) the channel number two monostable will be triggered causing its output to go HIGH and hence forcing the "W" output of the 74151 LOW as shown. The sequence explained above is repeated causing the 7493 to be incremented and the D3 data input to be sensed at "W" and so on. Figure 8 shows the output from this sequence at the "MUX" 74123 "Q" output. Note there is no pulse being generated to signify the end of channel number eight's quasistable time. In order to generate this end pulse (EP), the $\overline{Q}$ output from number eight (refer to figure 6) is applied to the rise triggered input of the EP 74123 monostable whose quasistable time is also set to 250 μsec. Figure 9 depicts the pertinent waveforms for this procedure.

The "Q" outputs of the multivibrators (MUX and EP) are now applied to the NOR gate (7402). The output from one NOR gate is shown in figure 10a. Figure 10b shows the inverted output which is derived by applying the output "X" to both inputs of another NOR gate (four NOR gates are available in the 7402). Either of these outputs can now be used to pulse modulate a transmitter. The calculations for the various RC values are given in Appendix B.

One of the benefits with this design is that inverted outputs are available for keying the transmitter. The temperature range over which the 74XX TTL devices operate is from 0°C to +70°C (a range of -55°C to +125°C is available using 54XX TTL replacements at an added cost).

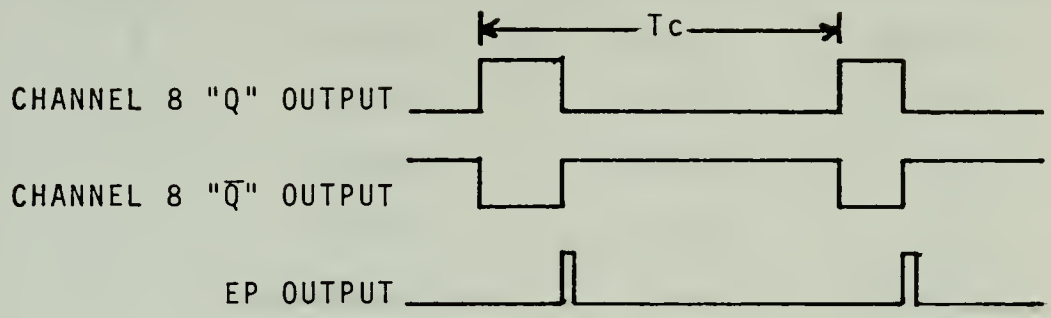


Figure 9. End Pulse Waveforms.

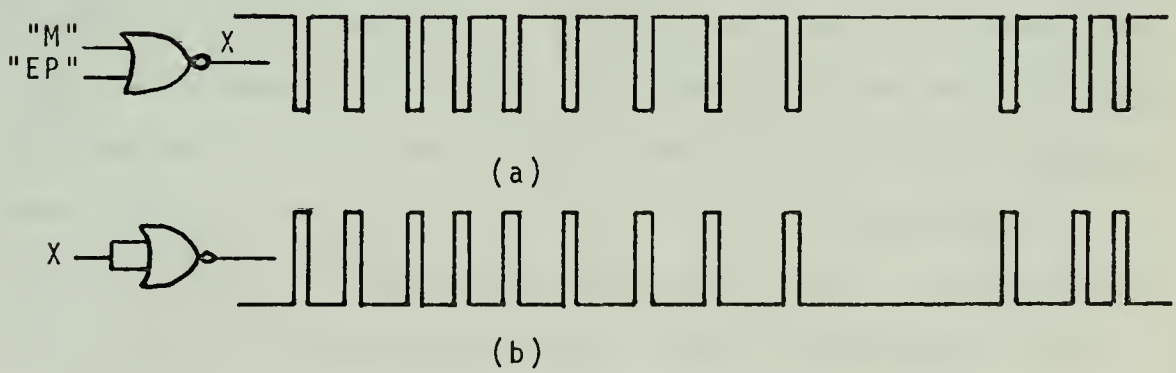


Figure 10. Time Multiplex Outputs: (a)inverted,(b)non-inverted.

The approximate cost breakdown for the components in an eight channel TTL encoder less sensors is given in Table II.

QUANTITY	DEVICE	UNIT PRICE	TOTAL PRICE
9	74123	$1.15	$10.35
1	74151	1.05	1.05
1	7493	1.05	1.05
1	7402	.25	.25
10	disc capacitors	.20	2.00
2	Rm	.10	.20
		TOTAL	$14.90

Table II. Cost Breakdown For TTL Encoder Components

One of the main drawbacks with this design is the amount of supply current required. Table III indicates a total of 684 mA max. This large current requirement restricts the use of small NiCad batteries for the aircraft power supply. Another slight drawback is that the 12 IC's and related R's and C's needed to fabricate eight channels are very difficult to package on a printed circuit board that is four inches by two inches. The encoder could however, be packaged on two printed circuit boards and placed one on top of each other. In view of the excessive current drain this encoder design was deemed unacceptable and a new method was pursued.

DEVICE	TYPICAL CURRENT(mA)	MAXIMUM CURRENT(mA)
7402	18	55
7493	32	53
74123	46ea.×8=368	66ea.×8=528
74151	29	48
TOTAL	447	684

Table III. Supply current required for TTL Encoder

B. LINEAR IC ENCODER

This second circuit was pursued with the intent of achieving a multi-channel encoder requiring a minimal current drain (less than 100mA if possible). The circuit uses Signetics NE/SE 555 Timers, 1N270 germanium diodes and associated resistor and capacitor components. N+1 timers and N diodes are required with N being the number of channels desired.[1]

Figure 11 depicts the overall circuit diagram for an eight channel encoder while figure 12 shows related waveforms for two channel operation. One 555, connected as a monostable multivibrator is required for each channel and an additional 555 is used to achieve the time multiplexing.

The input timing (or clock) is derived from control circuitry in the aircraft in the manner described for the TTL encoder. The input clock pulse is differentiated by RiCi

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[1] Signetics has recently produced a 556 Timer which is one IC package containing two-555 Timers. This will allow denser packaging.

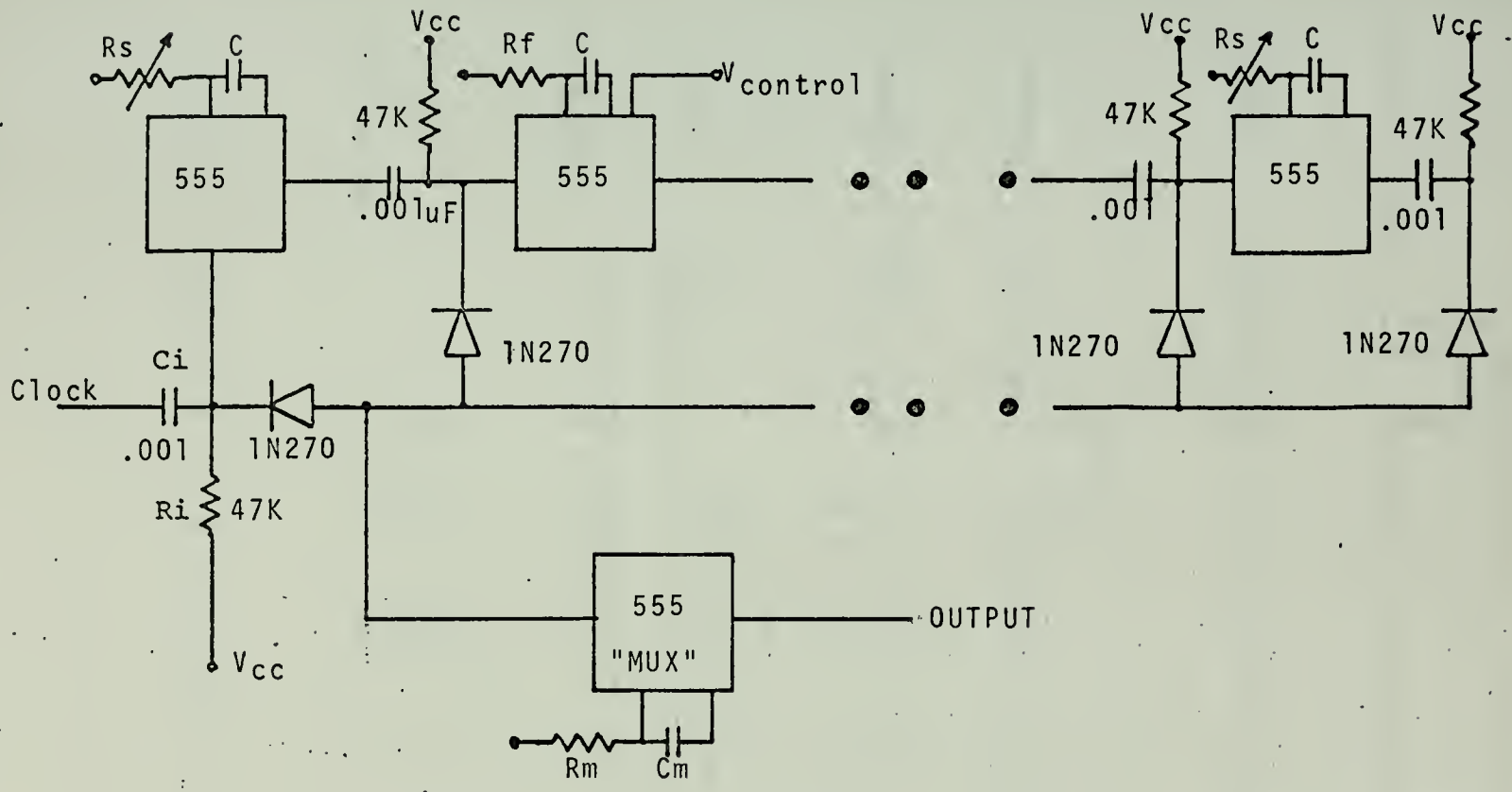


Figure 11. Linear IC Encoder Diagram.

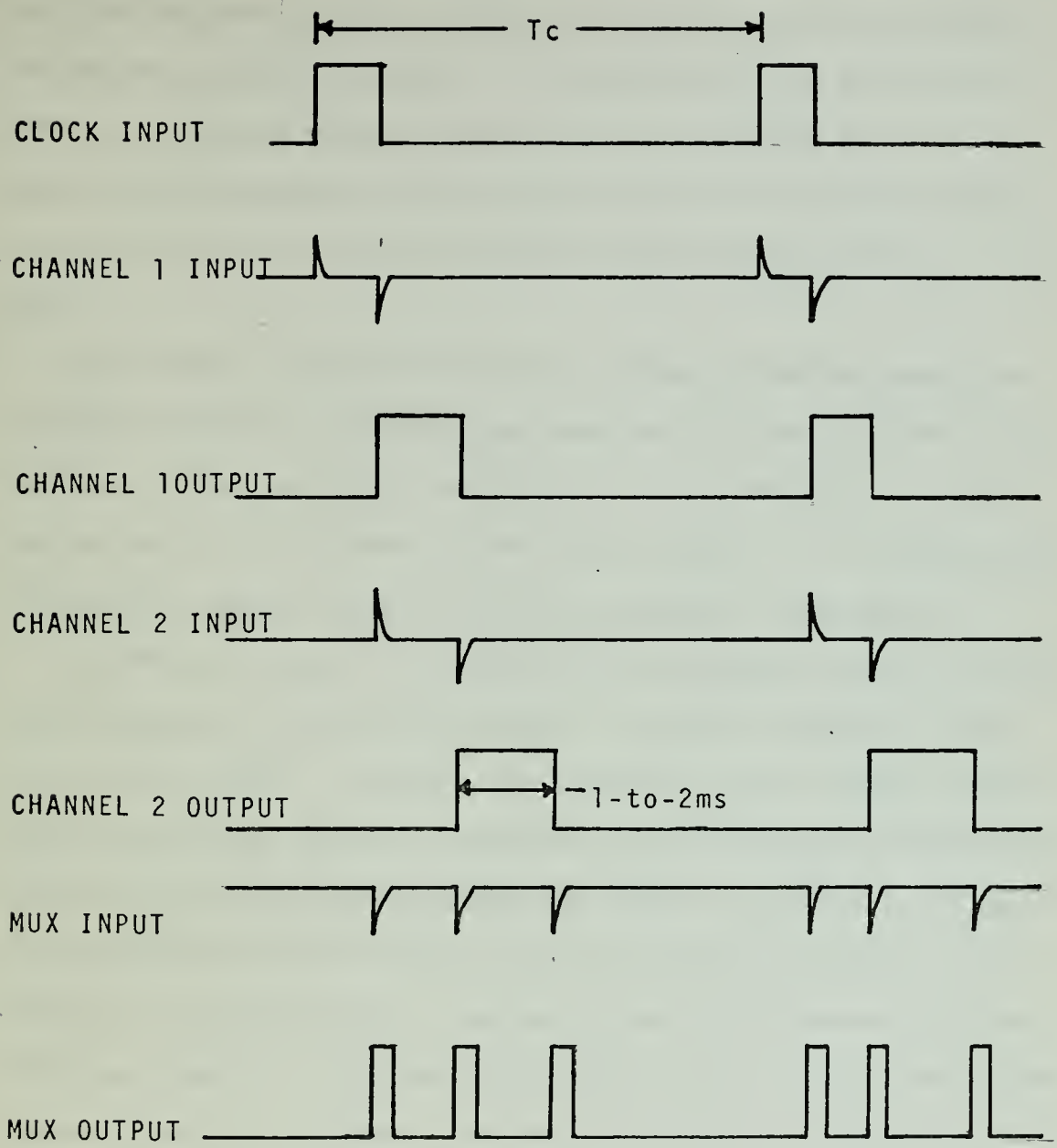


Figure 12. Waveforms for a Two Channel Linear Encoder.

(to prevent triggering on the positive transition of the logic type trigger signal) and applied simultaneously to the negative sensitive triggers of the channel one and MUX 555 Timers. Channel number one's output then goes HIGH for a period of time determined by Rs and C. The MUX 555 output also goes HIGH for 250 μsec (this time being fixed by Rm and Cm).

The output from channel one is then differentiated and applied simultaneously to the negative triggers of the channel two 555 as well as the MUX 555. This sequence is repeated until all channels have been sampled. The application of another input pulse starts the sequence over again.

If eight channels are used and the maximum "on" time for each channel is two milliseconds, the total sampling time required is 16ms. In order to achieve a sync time of three milliseconds or greater (required for the decoder circuitry), the clock repetition rate must be 19ms or greater. If this is not possible (some Radio Control systems use 17ms frame rates), than the sample time range for each channel can be adjusted down to 0.5-1.5ms which would give a total max frame rate of (8)(1.5)+3=15ms. To avoid interference between adjacent channels the minimum sample time must be greater than the multiplex pulse being generated (normally around 250 μsec). The above applies to the TTL encoder as well.

Referring to figure 11, notice that the 555 Timer for channel two has a pin labeled Vcontrol. This means that its quasistable time will be proportional to a varying input

voltage (see Appendix B for voltage versus time relationships). This feature allows for direct interfacing of sensors with voltage outputs.

This design has an approximate current drain of 60mA max (for eight channels) with Vcc=5Vdc. The timing error of an NE 555 is typically 1% with the external resistor value between one kΩ and 100kΩ. There is also a similar timing error associated with supply voltage drift and temperature variations. These errors should be insignificant due to the intended flight duration and altitude variation the model will experience; however, if actual operation proves otherwise, the supply voltage could be easily regulated and the more expensive SE 555 used. The SE 555 Timer is mil spec and the timing errors are lower.

It should be noted that this encoder design (as well as the TTL design) is non-linear in that timing is dependent on the charging of a capacitor. This means that output HIGH time is not linear with changes in Rs. Linearity can be achieved by having the capacitor charge through a constant current source. The circuit configuration and derivation for the time interval with a current source is given in Appendix B. The sacrifice for the linearity is the addition of an extra transistor and two resistors for each channel. This additional circuitry makes it extremely difficult to package these encoders in the space allowed in the aircraft.

National markets a linear timer IC (LM 3905) which is similar to the 555 in operation with the exception that the

input has a rise trigger and there is no need for differentiating the input pulses, hence one resistor and one capacitor may be eliminated for each channel. The only disadvantage is that the LM 3905 does not have provision for a Vcontrol input which means that additional interface circuitry would be required if a transducer with voltage output must be used.

C. DIGITAL/LINEAR ENCODER

Further design efforts resulted in an encoder circuit which was far superior to the previously described encoders. Up to nine channels may be synthesized using only four IC's and several external components (plus sensors). The IC's used are: a Signetics 555 Timer, a Signetics N7490 Decade Counter, a Signetics N74145 BCD-to-Decimal Decoder/Driver with Open Collector High Voltage Outputs, and a National 7432 Quadruple 2-input OR gate. The circuit diagram for this encoder is shown in figure 13.

The 555 is configured for astable operation. Diode D1 permits independent charge and discharge times for capacitor C. To be more specific, C will charge toward Vcc through Ra and D1. When the capacitor voltage reaches 2/3Vcc, the capacitor will discharge via transistor Q1 and resistors Re and Rs (the particular Rs depending on which output of the 74145 is tied to ground). The output of the 555 is HIGH during the charging period (fixed at 250 μsec) and LOW during the discharge period. Transistor Q1 along with diode D2 and resistors R1, R2, Re, and Rs form a constant current sink allowing

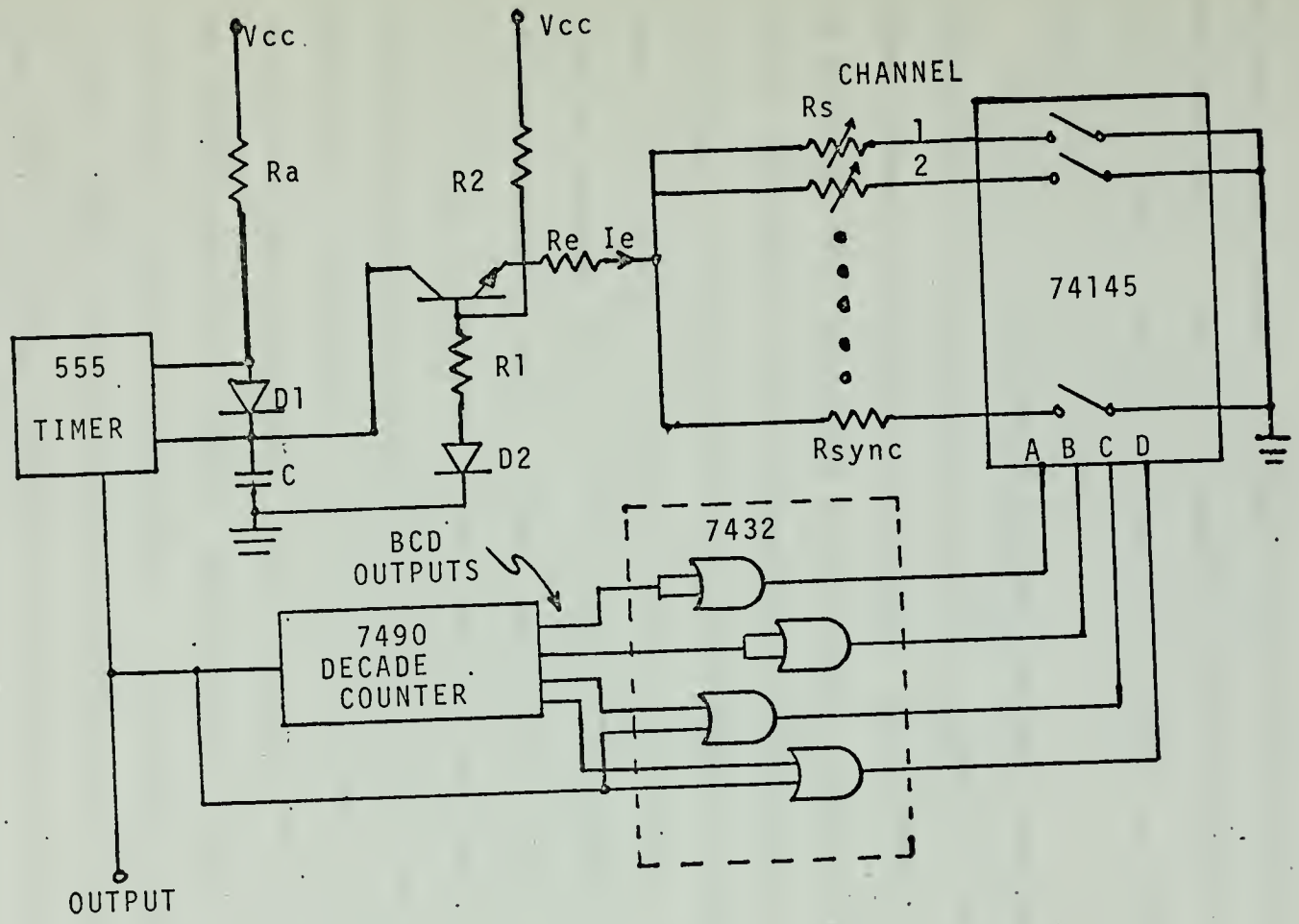


Figure 13. Digital/Linear IC Encoder.

the discharge time to vary linearly with the relation (derivation in Appendix B):

$$t(ms) = \frac{1/3Vcc(C)(Re)(R1+R2)}{Vcc-.3(R1)}$$

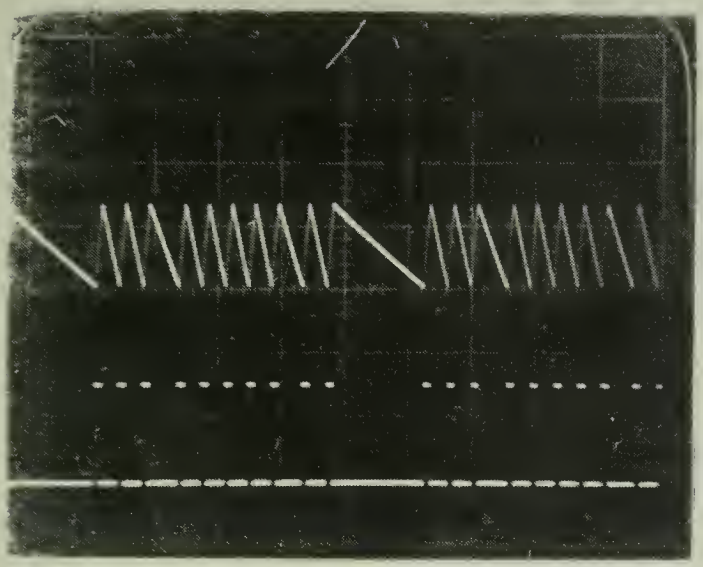
As previously noted, a linear system with minimal circuitry was desirable. The other encoders needed several constant current sinks to achieve linearity whereas this design requires only one such device.

In order to understand how the encoder functions, one may assume that the 7490 counter has some number in its registers. This number will appear at the output in BCD format via the OR gates to the BCD inputs of the 74145. This BCD input then causes the decimal related open collector output to be switched to ground. The 7490 counter is incremented by a fall triggered pulse which is obtained from the 555 output. As an example, assume that the 7490 contains the number one (i.e. its BCD output is 0001). This causes the decimal one output of the 74145 to go LOW. Since the 7490 was incremented to hold the BCD number one via the fall trigger from the 555, capacitor C also starts its linear discharge through transistor Q1 and the appropriate channel sensor. When the capacitor voltage falls to 1/3Vcc, the 555 output goes HIGH and capacitor C starts to charge anew. When the capacitor voltage reaches 2/3Vcc, the 555 output goes LOW again incrementing the 7490 by one count and grounding the next 74145 decimal output. This allows the capacitor to discharge via the next channel sensor (remember the 555 output is low during this

time). This process is repeated until all ten decimal outputs of the 74145 have been sampled at which time the 7490 decade counter starts over again. Only nine data channels can be generated because the tenth channel must be used to achieve the desired sync time (i.e. a fixed resistance replaces the sensor resistance Rs).

The purpose of the 7432 is to ensure that the charge times are dependent only on Ra and C as this time is included in total channel time. Observe that the 555 output is also tied to two different 7432 OR gate inputs along with outputs "C" and "D" from the 7490. This circuit gives a "1" output for "C" and "D" whenever the 555 output goes HIGH, hence the 74145 BCD input will always be 12 or greater (11XX) during this time. The result of a BCD input of eleven or more to the 74145 is that all the decimal outputs will be HIGH (or open); hence C will charge solely via Ra and D. When the 555 output is LOW the "C" and "D" outputs from the 7432 will follow the input from the 7490. Outputs "A" and "B" from the 7490 have also been connected to the remaining two OR gates in the 7432. This is done merely to allow outputs "A" and "B" to experience the same delay as outputs "C" and "D" and hence avoid any race problems. Figure 14 shows the related waveforms for the entire encoder process.

It is felt that this encoder design is superior to the previous encoders for several reasons: 1) this encoder is capable of generating more channels with fewer IC's and other external components in a smaller package, 2) the various



a) Upper Trace:
Capacitor
Waveforms

Lower Trace:
Multiplexed
Output

b) Exponential Rise
and Linear Decay
of Voltage Across
C.

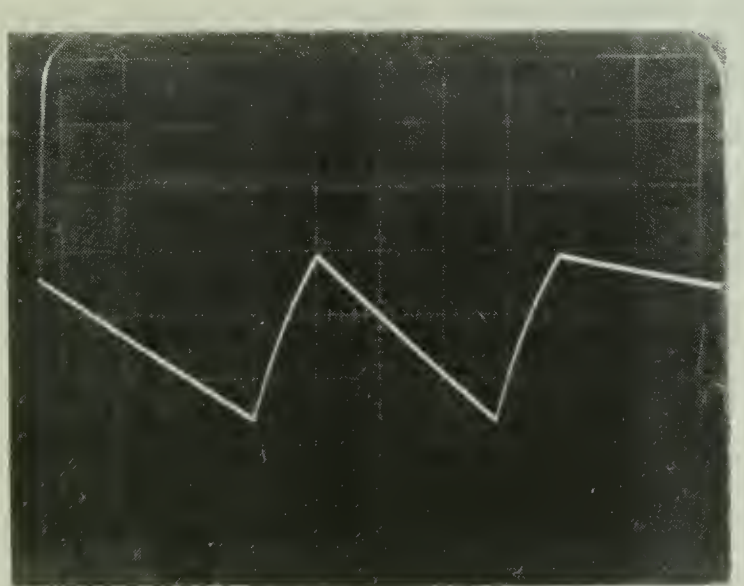


Figure 14. Related Encoder Waveforms

encoder output times can be made linearly proportional to sensor outputs with little difficulty, 3) there is a built in "failsafe" available in the event one or more of the sensors experiences a "glitch" or in the event a sensor is momentarily disconnected. At first glance one might think that if a failure (as noted above) did occur, there would be no path for C to discharge; however, closer inspection reveals that C would discharge through the combined leakage of the capacitor, diode D1, the constant current transistor and finite current drawn by the 555 voltage comparator circuitry. This discharge time has been observed to be approximately 40ms. The remainder of the data channel outputs are unaffected by this delay. Finally, 4) this design also generates its own clock, hence there is no need to rely on obtaining a clock signal from the aircraft avionics package. The typical current drain for this encoder, while not as low as the linear encoder, is an acceptable 110mA as shown in Table IV. Measurements taken with the actual circuit indicated an average current drain of 100mA. Perhaps the only disadvantage with this design is the requirement for interface circuitry if sensors with potentiometric outputs can not be obtained. In any event, the output pulse widths are varied by changing Ie. In the case of a voltage output all that would be required would be an FET which may be operated as a voltage controlled resistance. It should, however, be evident that the sensors should be obtained prior to choosing timing capacitors and fixed timing resistors (Ra for example) so their ranges can

be made compatible. Knowing the ranges, one may specify the remaining timing elements to achieve the 1-2ms pulse widths.

IC	SUPPLY CURRENT typ (mA)	max (mA)	COST
7490	32	53	$1.05
7432	32	55	.25
74145	43	70	1.45
555	3	6	1.00
Total	110	184	$3.75

Table IV. Encoder IC Current Requirements and Cost Breakdown

In conclusion, this encoder was chosen over the previous designs because it best satisfied the system requirements for size, weight, low power drain and cost, accuracy and reliability.

III. DECODER DESIGN

The decoder consists of two IC's and two external components. It is compatible with all of the encoders described in section II. The IC's are one each Signetics N8273 10-bit serial-in, parallel out shift register, and one each Fairchild TTμL 9601 retriggerable monostable multivibrator.

The pulse train that arrives at the "P" input in figure 15 is similar to the outputs from the various encoders with the exception that this circuit will accept from one to ten channels and requires a sync time greater than the time constant RsCs. The pulse train is applied simultaneously to both the rise-triggered clock input of the 8273 and the fall triggered input of the 9601. This causes the 8273 to "shift" 250 μsec prior to the 9601 being triggered. The 9601 is adjusted for a quasi-stable period (tq) that is: 2.5ms<tq<sync time. The $\overline{Q}$ or normally high output of the 9601 drives the serial input (D) of the 8273.

The easiest way to explain how the decoder functions would be to go through a few frames of input pulses. Assume that the applied pulse train is at the end of a sync pause. The 8273 is empty (i.e. all outputs low) and the 9601 is in its stable state ($\overline{Q}$ output high). The leading edge of the first pulse arrives clocking a "1" into the first output channel (i.e. channel number one's output goes HIGH). After 250 μsec, the first input pulse terminates. This triggers the 9601 to its quasi-stable state. At the end of channel

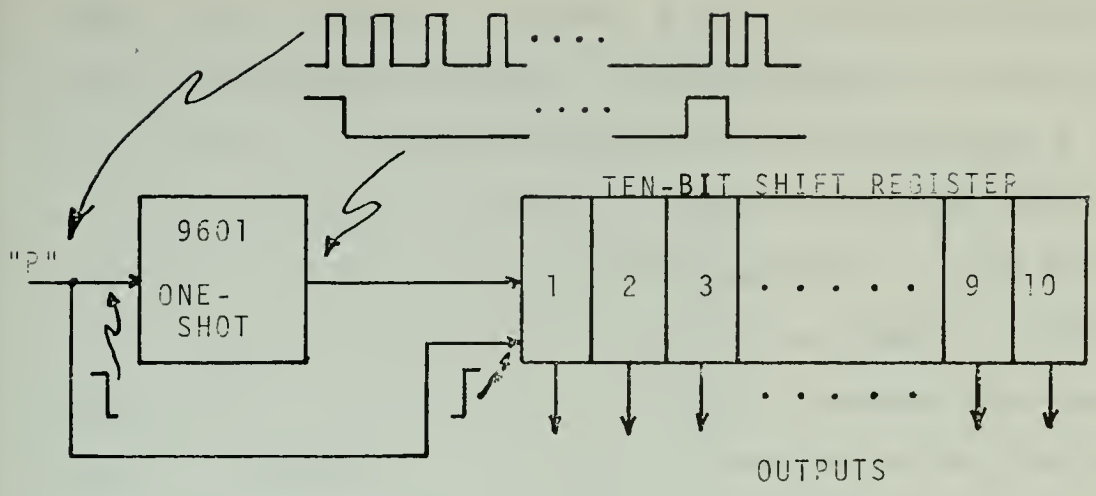


Figure 15. Decoder Diagram.

a) Upper Trace:

9601 $\overline{Q}$ output

b) Lower Trace:

pulse train input

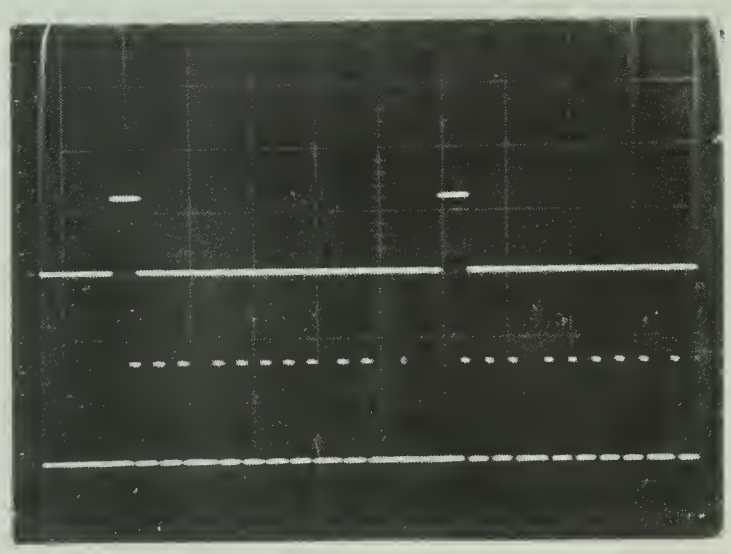


Figure 16. Decoder Waveforms

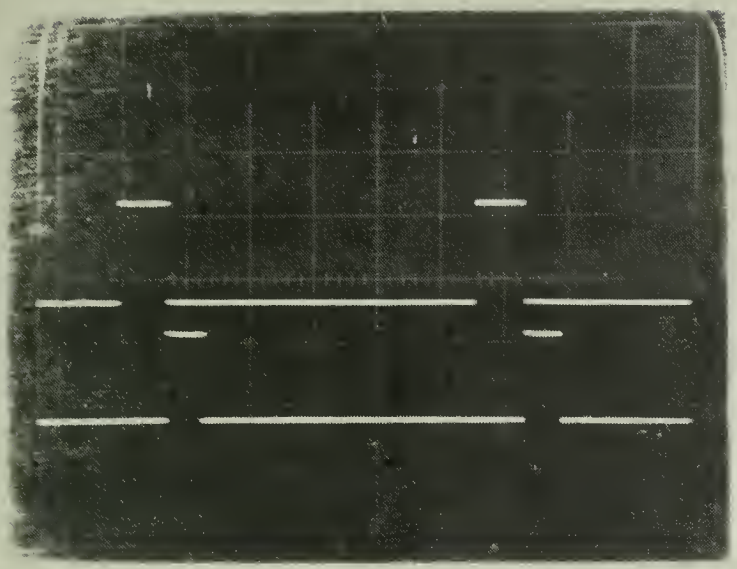
number one's data time (between 1-2ms) the second control pulse arrives shifting the "1" into the second output channel of the 8273 and, since the 9601 has not yet relaxed, a "0" is placed in channel number one. At the trailing edge of pulse two, the 9601 is retriggered again for a time equal to "tq". Each pulse thus shifts the "1" one channel further down the 8273 until the ten (or fewer) channels have been received. Following the channel information is the sync pause which, since it is greater than "tq", allows the 9601 to relax and set up the serial input of the 8273 (Tset-up=15ns) with a "1" to start the sequence anew with the first pulse of the next frame. Figures 16 and 17 illustrate the related waveforms for the decoder operation as described above.

If the control sequence is less than ten channels, the outputs downstream of the controlled channels are a repetition of the control sequence. It is never necessary to clear the 8273 because the unused data is continuously being dumped to the non-used outputs of the shift register.

In the event that a frame of data is not received or a "glitch" causes an errant signal to be generated, the decoder will resynchronize with the start of the next frame.

It should now be evident that the mere changing of RsCs is all that is required to make the decoder compatible with any of the previously described encoder designs.

Table V lists the cost breakdown for the decoder components.



a) Two simultaneous channel outputs

b) channel three output (upper)

input pulse train (lower)

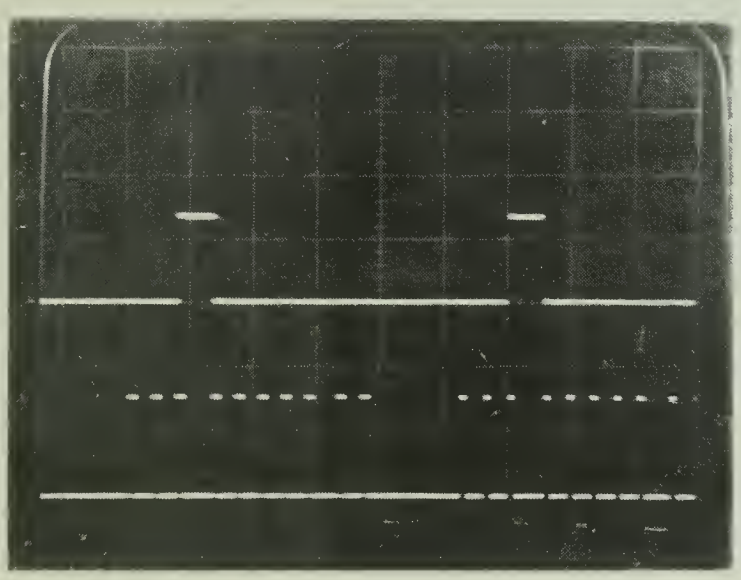


Figure 17. Decoder Waveforms

COMPONENT	COST
9601	$1.15
8273	3.00
Rs	.10
Cs	.25
TOTAL	$4.50

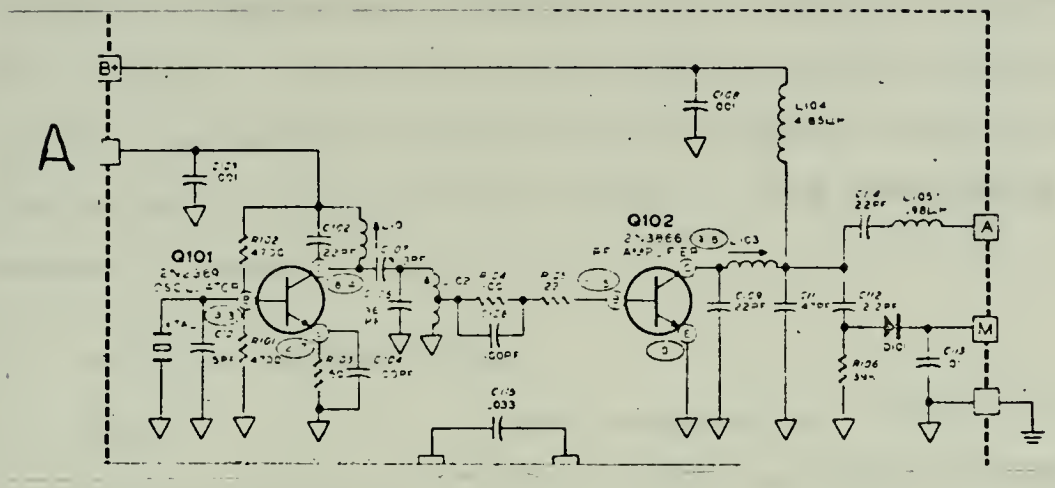
Table V. Decoder Component Costs

IV. OTHER SYSTEM CONSIDERATIONS

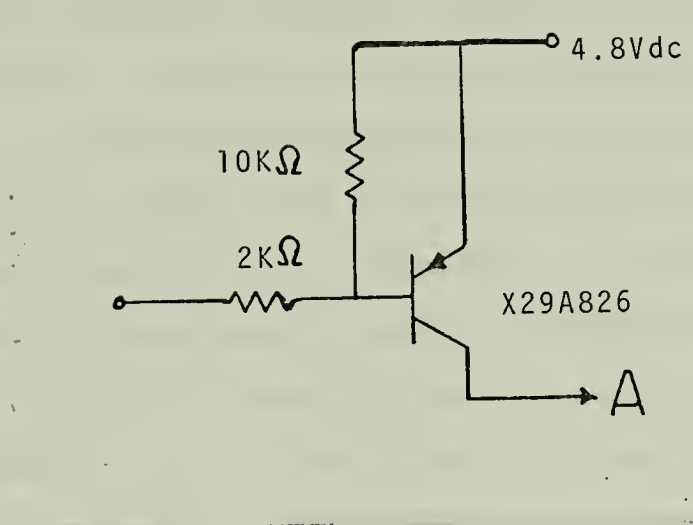
The transmitter and receiver had little bearing on the design work involved with the thesis because these items were already available commercially. The following paragraphs will focus on the interfacing requirements for the transmitter and receiver with the telemetry system rather than detailed circuit descriptions. The final section deals with readout devices that might be used.

A. TRANSMITTER CONSIDERATIONS

The main problem encountered in selecting a transmitter was determining what frequencies could be used. The available frequency bands for flying models are 27MHz, 54MHz, and 72MHz. The FCC prohibits downlinks on the 27MHz and 72MHz bands hence the downlink frequency was chosen as 54MHz. Actually, any of these frequencies would be usuable if the RF output power is kept below 100mW. Although 100mW would provide the range required, it was still decided to use 54MHz because Heathkit sold an RF transmitter board for $10 and more power was available if desired. The Heathkit transmitter schematic is shown in figure 18. The RF output power is 400mW into a 50Ω load with an approximate 100mA current drain for Vdc=9.6. The RF board must be reconfigured somewhat in order that size constraints are met and the circuit must be optimized and retuned for 4.8 volt bias. The only other addition is one transistor and associated resistors to provide the interfacing

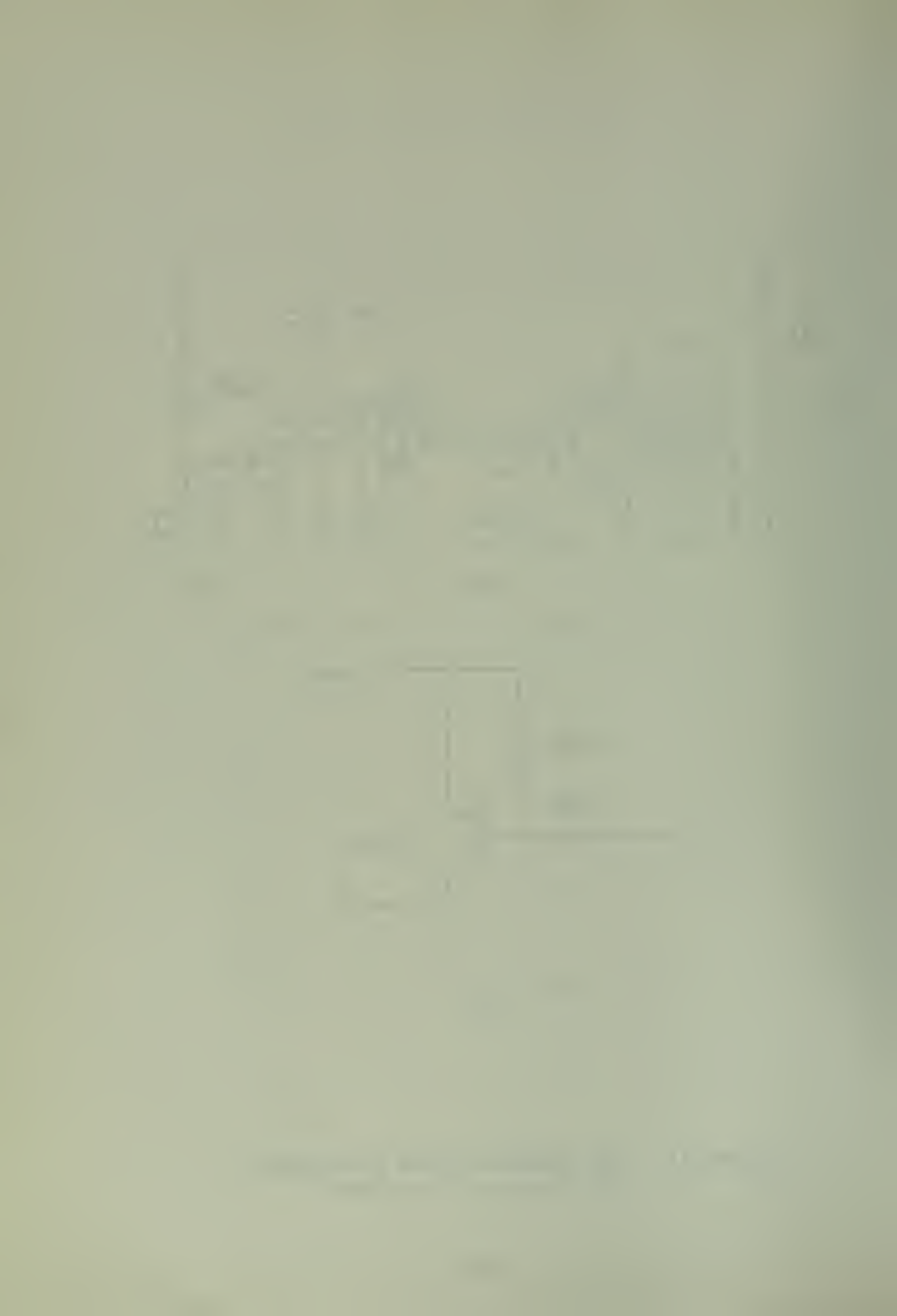


(a)



(b)

Figure 18. (a) Heathkit 54MHz Transmitter,
(b) Interface Circuitry

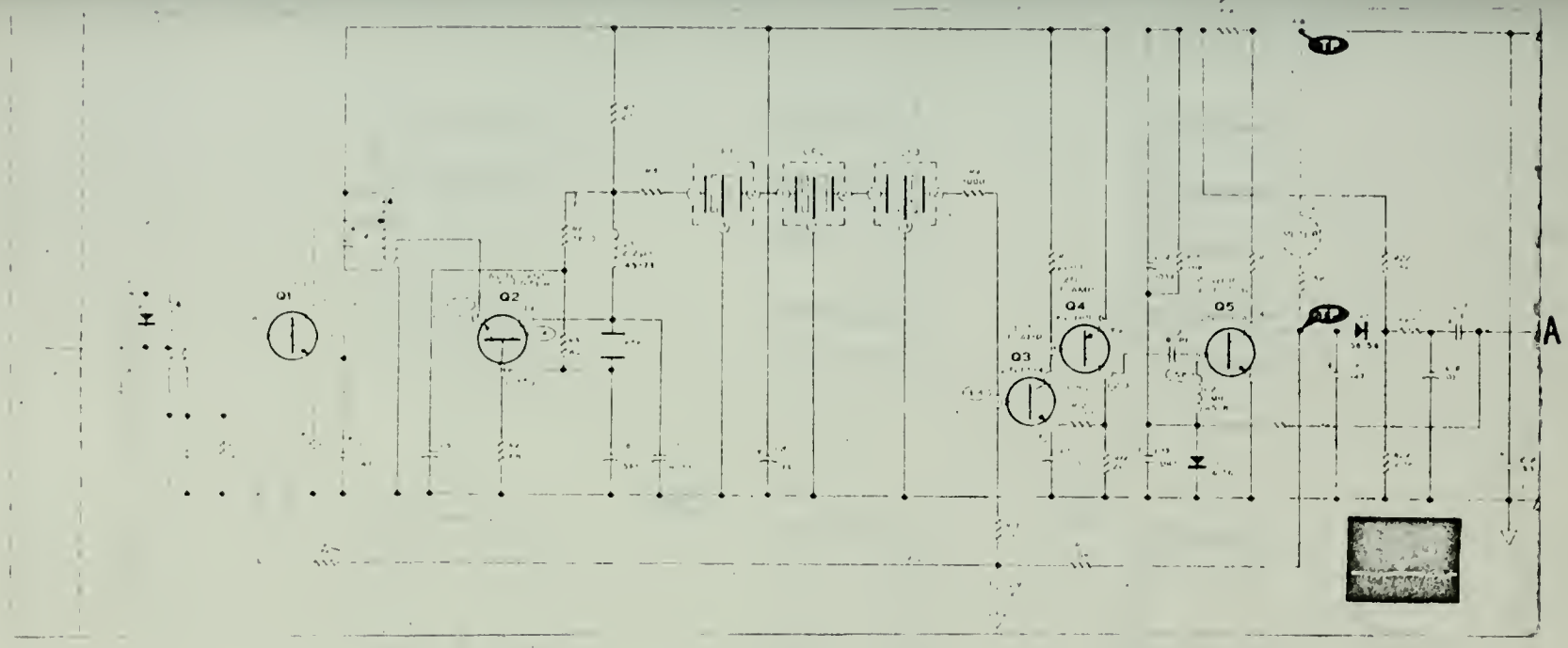


required for the encoder to modulate the transmitter. These modifications are neither expensive nor time consuming.

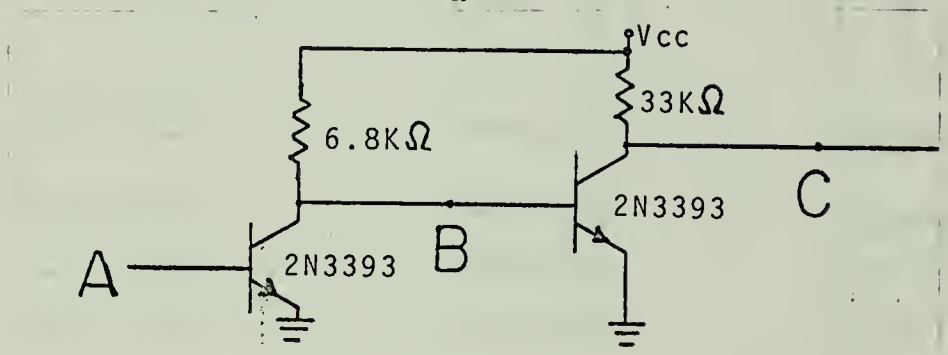
The transmitter consists of a crystal oscillator transistor (Q101) and a final RF amplifier transistor (Q102). The encoder output drives a PNP transistor which has two functions: 1) it inverts the encoder pulses and 2) provides enough current to ensure that the oscillator transistor operates during the interval between 250 μsec pulses. This interfacing transistor is shown in figure 18b.

B. RECEIVER CONSIDERATIONS

The front end of any 54MHz receiver would adequately receive the transmitted signal but once again cost, as well as compatibility considerations proved the deciding factor in choosing a Heathkit receiver available for $35. The receiver consists of a conventional crystal-controlled superheterodyne front end with pulse amplifying and integrating circuitry and a separate pc board with decoder circuitry for three channels of fixed frame data. The receiver is packaged such that the receiver pc board can be operated independently from the decoder circuits. Figure 19 shows the schematic diagram for the portion of the circuit used with the telemetry system. In order to obtain a signal that will properly drive the telemetry decoder, transistors Q1 and Q2 are required. These transistors can be taken off the decoder circuit board that comes with the receiver. The significant received waveforms are illustrated in figure 20. The waveform at point A is inverted by Q1 and amplified sufficiently to drive Q2. When



a



b

Figure 19. a) Heathkit 54MHz Receiver, b) Decoder Interface Circuitry

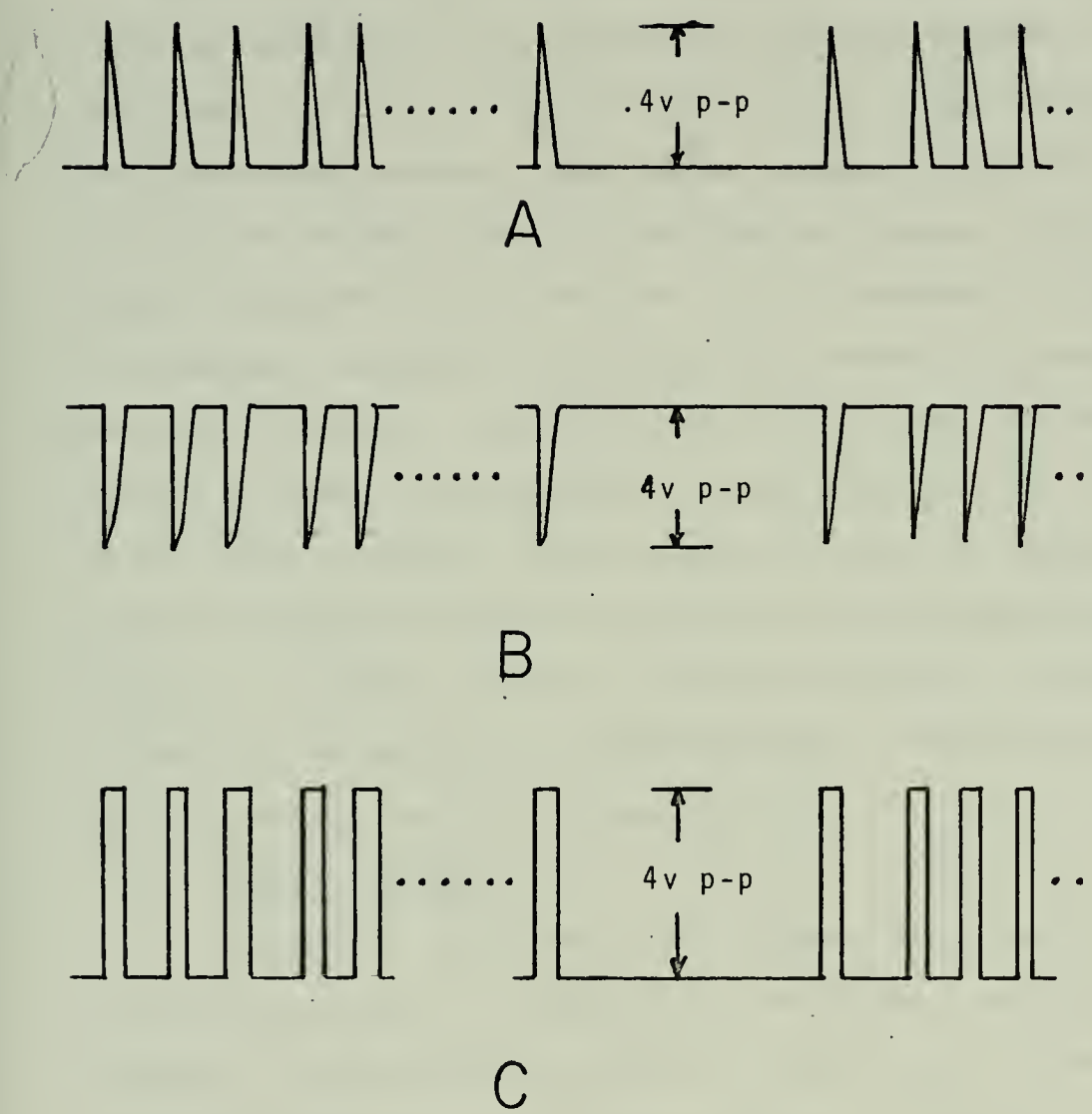


Figure 20. Receiver Waveforms.

Q2's base drops below approximately 0.6Vdc Q2 shuts off causing the collector to rise to 4Vdc thus providing a pulse train of proper amplitude and polarity to drive the decoder.

C. READOUT DEVICES

Before choosing a particular type of display, it is imperative to understand a significant difference between a system employing the TTL or Linear Encoder and a system with the Digital/Linear Encoder. The former encoders operate in a synchronous manner, that is, the decoded channel outputs are always separated by a fixed time. This assumes that the clock signal from the aircraft control system is fixed.[2] The latter encoder is asynchronous in that the individual channel outputs are separated by times that vary as a function of the other channels. This means that similar readout devices or techniques cannot be used with the linear/digital encoder. In view of the fact that this encoder is better suited for the application desired here, a discussion of compatible readout devices is appropriate.

1. Servo Readout

Figure 21 shows the block diagram for a typical servo control unit which is commercially available from Heathkit Company. The servos translate the signal pulses from the individual channel outputs into positive or negative voltages that drive a motor. The motor shaft is coupled to linear and

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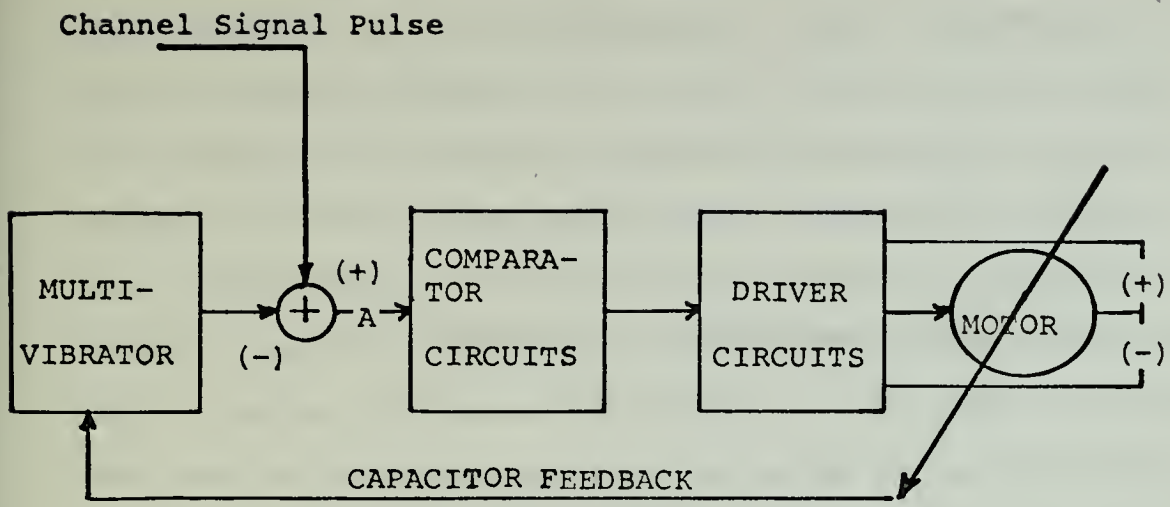
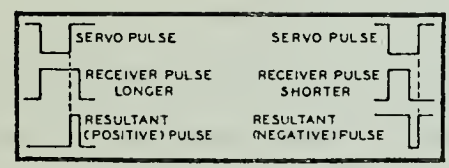
[2] The majority of Remote Control systems commercially available for model control are fixed frame rate systems.



(a)



(b)

Figure 21. Typical Servo Unit, (a) Block Diagram (b) Waveforms

rotary rack gears as well as a variable capacitor that controls feedback to the multivibrator. When a difference signal is sensed (at point A) the motor drives the rack gears. As the gear train turns the capacitor plates turn such that the multivibrator output pulse width matches the incoming signal pulse width. Because the two pulses are opposite in polarity (equal in amplitude) there is no longer a difference pulse to drive the motor. The servo unit is directly compatible with the decoder circuitry explained in section III because a) the servo operates with a channel signal level of approximately three volts which is similar to typical output levels from the 8273 shift register and b) the servo was designed for use with radio control equipments where the channel pulses vary from one-two milliseconds.

The servo unit receives power from a 4.8Vdc supply making it ideal for field work. The rotary wheel output can be used to position an indicator over a range of approximately 100 degrees.

2. Digital-to-Analog Readout

The following was designed to take the channel outputs from the decoder and provide a voltage output proportional to the channel pulse widths. The circuit is configured with the following IC's: Signetics 555 Timer, N7404 Hex Inverter, 74279 Quadruple $\overline{S}$-$\overline{R}$ Latches, uA741 Op Amps, and National DM7552 Decade Counters with Latches.

The 555 functions as the system clock. The various channel counters are incremented by the clock pulses whenever

the proper channel output pulse is present. The clock rate is set at 100 pulses/ms (this gives 1% accuracy), hence if a decoder pulse is HIGH for .5ms the counters would hold the BCD number 50. The BCD counter outputs are then fed to a weighted resistance ladder which, in turn, form the input resistance for the Op Amp. The Op Amp drives a meter movement such that the output voltage is directly related to the BCD number stored in a channel counter. If two counters are cascaded any number from 0-99 can be accumulated. Since the channel outputs vary from one-to-two milliseconds, a minimum of 100 counts will always be received. After 100 pulses are counted, a terminal count (TC) is generated and the counters will start over at zero and count up to 99 depending on the pulse width of the input.

The actual operation of the circuit is best described with the aid of the timing and block diagrams of figures 22 and 23. Assume that channel three had the BCD number 88 stored in its counter when channel one's output goes HIGH. After 100ms the TC output from channel one's counter is generated. This pulse is then inverted (via the 7404) and tied to the $\overline{R3}$ input of the 74279. This drives Q3 low causing the latches in channel three's counter to "lock" up. The data paths between the counter outputs and the BCD outputs are now inhibited. This means that the BCD number 88 is locked in buffer registers even though the counters and respective TC outputs are still operable. After channel two has been on for one millisecond, its TC pulse is generated clearing

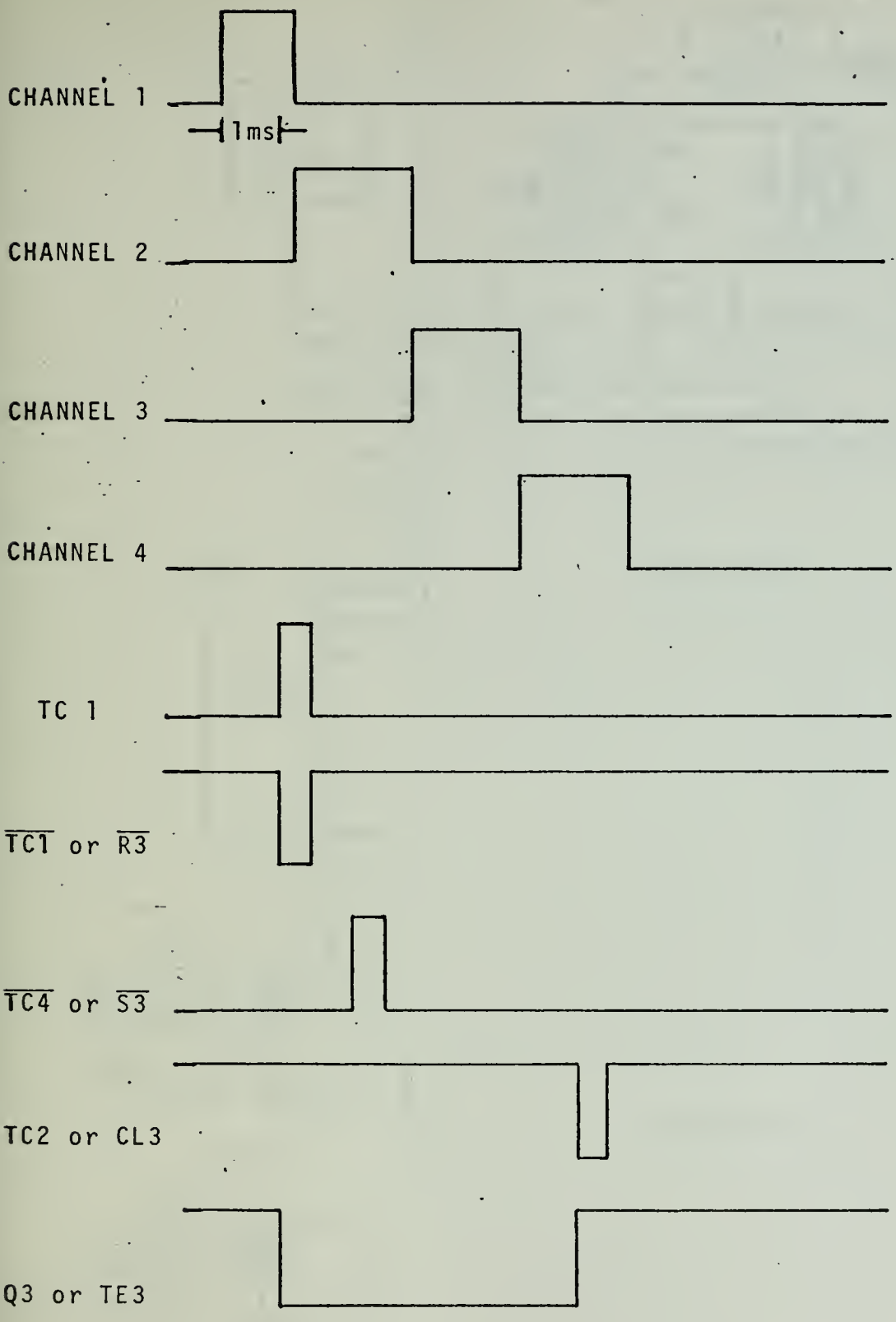


Figure 22. D-A Timing Diagram.

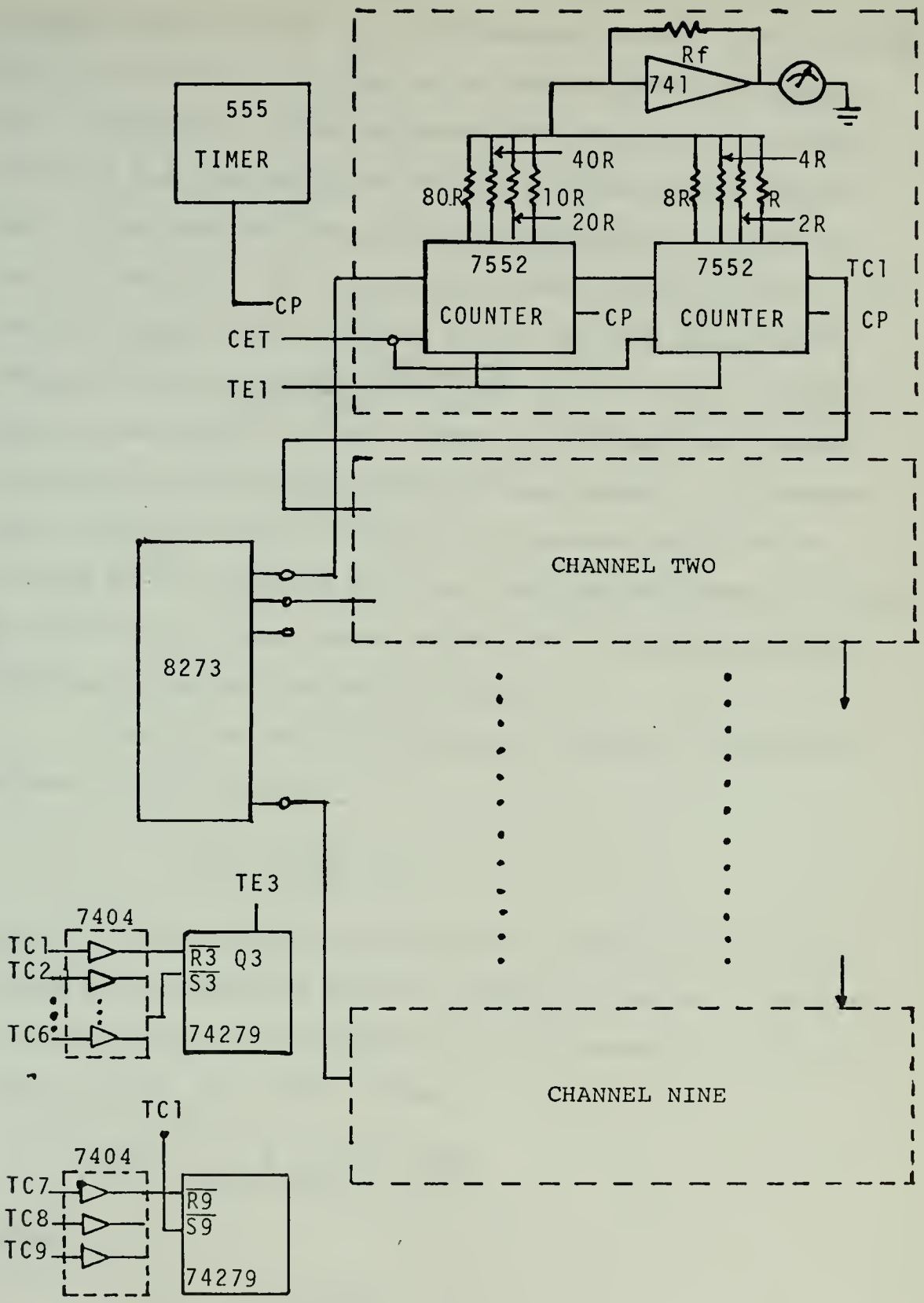


Figure 23. Digital-to-Analog Readout Device.

channel three's counter. Next channel three's input arrives and a new number is stored in its counter (the BCD outputs still contain 88). The TC pulse from channel four is then inverted and tied to $\overline{S3}$ of the 74279 causing Q3 to go back HIGH. This enables data transfer between the counters and the BCD outputs. If a count other than 88 was entered a new voltage appears at the output of the Op Amp. This timing sequence allows a number to be held in the output registers while a new sample is being taken. In effect four channels are used to provide the timing for one channel. If channel nine's operation were looked at its counter would be: a) latched by the inverted TC pulse from channel seven, b) cleared by the TC pulse from channel eight, and c) unlatched by the inverted TC pulse from channel one.

The Op Amp output voltage is related to the counter outputs by the equation:

$$Vout = \frac{-Rf}{Req} Vin$$

The value for Rf should be chosen so a desired Vout is obtained for the MAX Req from the resistance ladder. The maximum resistance is determined by the BCD number 99 (i.e. pins A_0, D_0, A_1, D_1 are HIGH). Then,

$$Req = \frac{1}{80R} + \frac{1}{10R} + \frac{1}{8R} + \frac{1}{R} = \frac{80R}{99}$$

hence

$$Rf = \frac{Vout}{Vin} \frac{80R}{99}$$

If the counter holds the BCD number 6, Vout is:

$$Vout = \frac{\frac{80R}{99}}{\frac{1}{40R}+\frac{1}{20R}} Vin = \frac{6}{99}Vin$$

or if the counters held the BCD number 47 then Vout is:

$$Vout = \frac{\frac{80R}{99}}{\frac{1}{80R}+\frac{1}{40R}+\frac{1}{20R}+\frac{1}{2R}}Vin = \frac{47}{99}Vin$$

V. TESTING OF THE PROTOTYPE

The following paragraphs refer to testing of the system using the Linear/Digital Encoder.

A. LINEARITY

In order to determine if the constant current source did yield a linear output from the encoder, two channels of the system were varied and the various output times plotted against the theoretical times obtained from the equations in Appendix B. In addition, the observed data was fit to a curve via the method of LEAST SQUARES and an empirical equation derived. Table VII in Appendix B lists the comparisons of actual and calculated output times.

The graph of figure 24 shows that a plot of calculated and observed outputs both follow a linear equation. The "offset" in both instances is due to the charge time (Tr) for the capacitor (which in this case was set to 200 μsec). The fact that the slopes of the two plots differs is attributable to the tolerances of components used and inconsistancies in supply voltage. The largest error is at Re=7KΩ where the percentage error is (2.18-1.95)/2.18=11%. This is very satisfactory considering ±10% resistor and capacitor tolerances as well as the aforementioned changes in Vcc or Vbe which would cause changes in the slope.

In conclusion, the above data indicates strongly that the constant current sink is indeed functioning as designed.

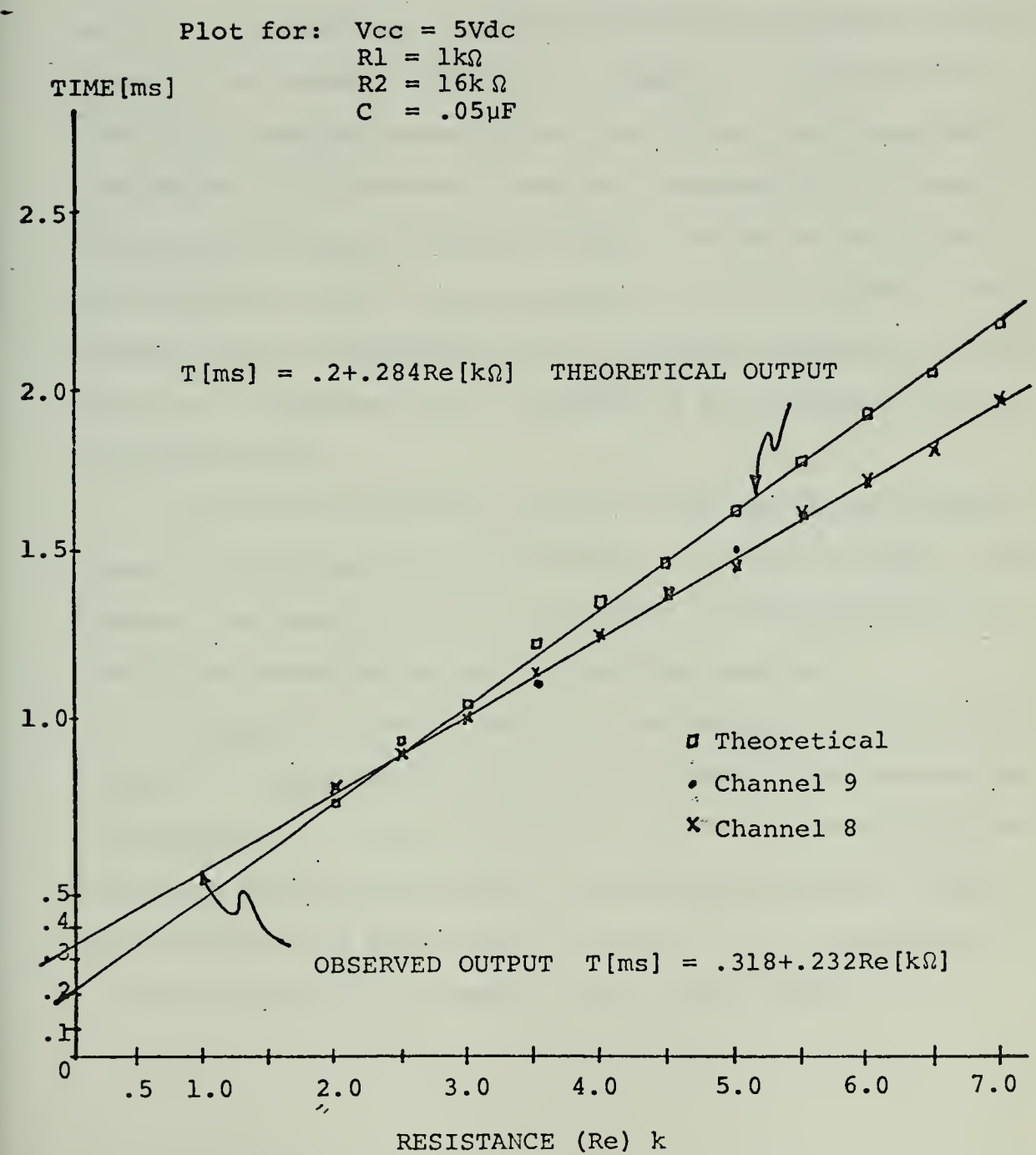


Figure 24. Observed versus Theoretical Encoder Outputs

B. RF LINK

After the entire system was breadboarded and checked for proper operation on a section by section basis (i.e. encoder circuits, decoder circuit etc.) it was important to demonstrate that the system components functioned properly as a unit. Of particular importance was the performance of the encoder and decoder IC's in the presence of an RF field. In addition, decoded output pulse width times were observed to determine if the accuracy remained comparable with results obtained previously with the encoder output wired directly to the decoder input. The transmitter was not retuned or reconfigured hence measurements such as output RF power or range were not considered. The transducers were simulated using potentiometers.

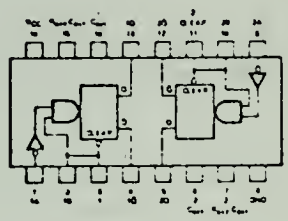
The system functioned properly with the RF environment apparently having no effect on the IC's in the system. The channel pulsewidths from the decoder followed exactly the empirical equation derived in the last section.

Although the system functions as desired, further tests should be implemented after final packaging and transmitter optimization to check if there is any significant difference with the output pulsewidths in a noisy environment (both mechanically and electrically) such as will be encountered in the model RPV as a result of the engine used.

APPENDIX A

PERTINENT DATA ON INTEGRATED CIRCUITS

Signetics N74123 Retriggerable Monostable Multivibrator



†Pin assignments for these circuits are the same for all packages.

Figure 25. Pin Configuration

S54123,N74123

INPUTS		OUTPUTS	
A	B	Q	$\bar{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎎
↓	H	⎍	⎎

Figure 26. Truth Table

Notes: H = high level

L = low level

↑ = transition from low to high level

↓ = transition from high to low level

X = any input

Signetics N74151 8-line to 1-line Data Selector/Multiplexer

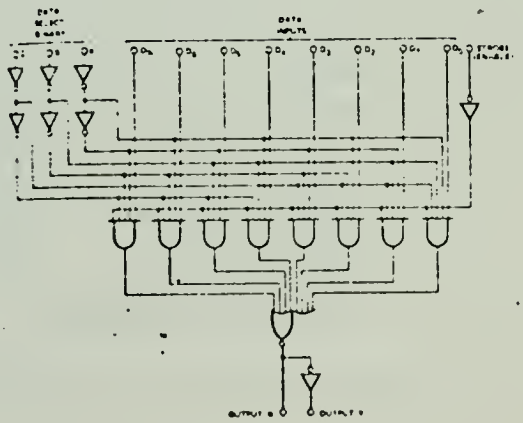


Figure 27. Logic Diagram

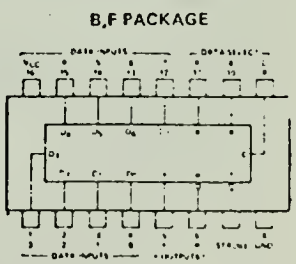


Figure 28. Package Data

Signetics 74151 continued.

INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

When used to indicate an input X = irrelevant.

Figure 29. Truth Table

Signetics NE/SE 555 Timer

Monostable Operation

Referring to the block diagram and the monostable configuration observe that capacitor C is held discharged by the transistor inside the 555. When the 555 receives a negative trigger, the flip-flop is set releasing the short across C

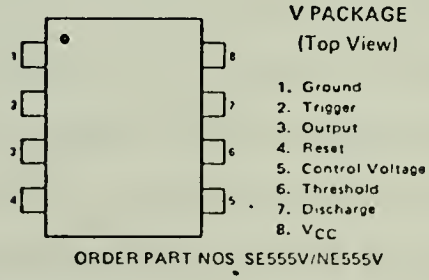


Figure 30. Package Data

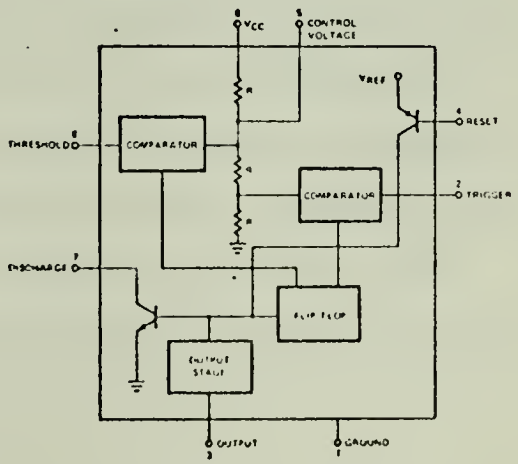


Figure 31. Block Diagram

and also driving the output HIGH until C has charged to 2/3 Vcc when the flip-flop is again reset via the comparator at pin six. The time that the output is in the HIGH state is given by

$$t_h = 1.1\ RaC$$

The High time may also be determined by applying a varying voltage at pin five. For this mode of operation, when triggered, the external capacitor will charge toward Vcontrol

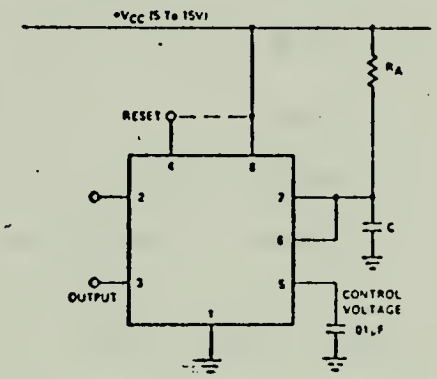


Figure 32. Monostable Configuration

through Ra. When Vcontrol is reached, the flip-flop will be reset (via the comparator) and the output goes LOW. The voltage across the capacitor still increases exponentially with a time constant equal to RaC but is only allowed to charge to the control voltage. Table VI shows observed output times (HIGH) versus control voltage over a range of one volt. The relationship between Vcontrol and output HIGH could be made linear by replacing Ra with a constant current source.

Vcontrol (V)	t_h (ms)		Δt (ms)
3.0	0.58		
		>	.03
3.1	0.61		
		>	.04
3.2	0.65		
		>	.04
3.3	0.69		
		>	.04
3.4	0.73		
		>	.05
3.5	0.78		
		>	.04
3.6	0.82		
		>	.06
3.7	0.88		
		>	.06
3.8	0.94		
		>	.06
3.9	1.00		
		>	.06
4.0	1.06		

note: Ra = 10kΩ, C = 0.1μF.

Table VI. Output time HIGH versus Vcontrol

Astable Operation

In this configuration, the 555 will trigger itself and run as a multivibrator. The external capacitor charges toward Vcc through Ra, Rb and C. When the voltage across C reaches 2/3 Vcc the comparator output resets the flip-flop driving

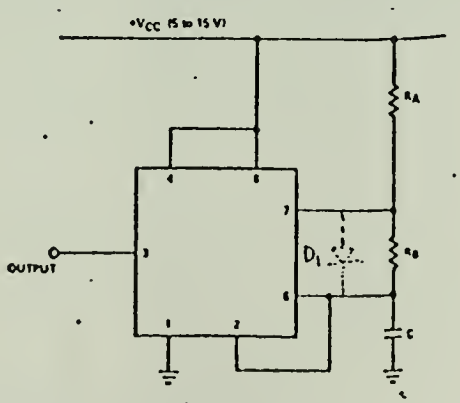


Figure 33. Astable Configuration

the output LOW and discharging C through Rb and the internal transistor. When the capacitor voltage falls to 1/3 Vcc the output of the comparator at pin two resets the flip-flop which starts the cycle over again (i.e. the output goes HIGH as C begins charging toward Vcc again).

The time the output is HIGH is given by

$$t_h = .693(Ra+Rb)C$$

and the time the output is LOW is given by

$$t_l = .693(Rb)C$$

Signetics N74145 BCD-TO-DECIMAL Decoder/Driver with Open Collector High Voltage Outputs.

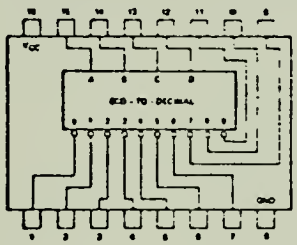


Figure 34. Pin Configuration

INPUTS			
D	C	B	A
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

OUTPUTS									
0	1	2	3	4	5	6	7	8	9
0	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1
1	1	1	1	0	1	1	1	1	1
1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	1	1	1
1	1	1	1	1	1	1	0	1	1
1	1	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

Figure 35. 74145 Truth Tables

Observe that if a diode is placed between pins six and seven as shown (dotted in figure) a 50% duty cycle may be achieved. The output times will now be

$$t_h = .693(Ra)C$$

$$t_l = .693(Rb)C$$

Signetics 8273 10-Bit Serial-In, Parallel-Out Shift Register

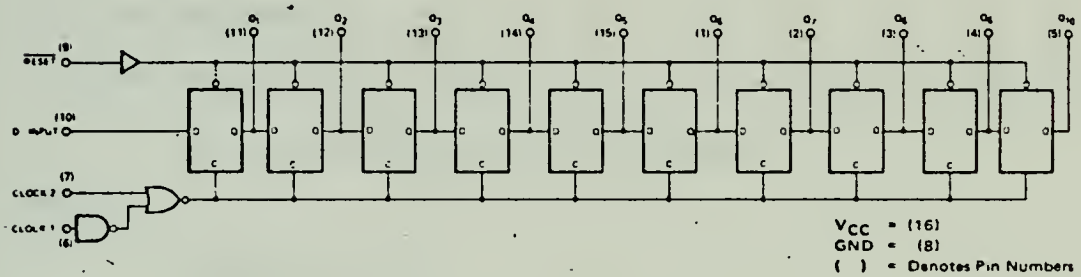


Figure 36. Logic Diagram

INPUT	$\overline{RESET}$	CLOCK 1	CLOCK 2	Q_{n+1}
1	1	Pulse	0	1
0	1	Pulse	0	0
1	1	1	Pulse	1
0	1	1	Pulse	0
1	1	Pulse	1	Q
0	1	Pulse	1	Q
1	1	0	Pulse	Q
0	1	0	Pulse	Q

NOTE The unused clock input performs the INHIBIT function

$\overline{RESET}$ = 0 > Q = 0

Figure 37. Truth Table

APPENDIX B

ASSOCIATED ENCODER/DECODER CALCULATIONS

The following is a list of calculations for the pulse widths associated with the various encoder designs described in section II.

1. TTL ENCODER

The output pulse width (t_w) for the 74123 is given by

$$t_w = 0.32 Rext Cext [1+(0.7/Rext)]$$

where:

Rext is in kΩ

Cext is in pF (Cext>1000pF)

t_w is in ns

Knowing that the pulse widths for each channel will vary between one and two milliseconds and assuming the transducer outputs have a range from 5-10kΩ (the 74123 external resistance must range between 5-50kΩ hence a fixed resistor would be required if a particular sensor cannot be obtained with the above range), one may solve for Cext.

$$Cext = \frac{\Delta t}{.32\ R[1+(.7/\Delta R)]}$$

where:

$\Delta t = 1ms = 10^6 ns$

$\Delta R = 5k\Omega$

$$Cext = \frac{10^6}{.32(5)(1+.14)} = 0.55\mu F$$

The same formula is used to obtain the values for the 250 μsec multiplex pulses.

2. LINEAR ENCODER

The pulse widths are the same as with the TTL encoder (i.e. Δt=1ms) and there is no restriction on the value for the external resistance with the 555 Timer.

For individual channels:

$$\Delta t = t_h = 1.1RaC$$

where:

$$\Delta t = 1ms$$

$$\Delta R = Ra = 5k\Omega$$

$$C = \frac{10^{-3}}{1.1(5)(1000)} = 0.18\mu F$$

For the Multiplex pulse widths:

$$\Delta t = 250\ \mu sec$$

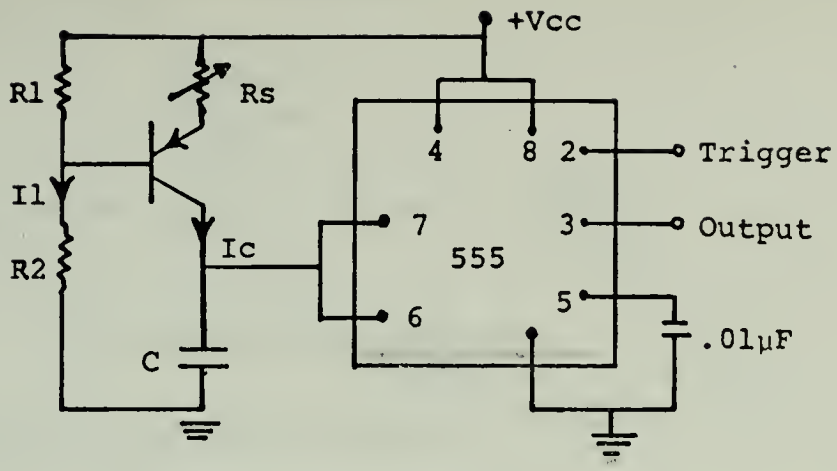
let C=.01μF then,

$$Ra = \frac{250\times10^{-6}}{1.1(.01)(10^{-6})} = 22.7k\Omega$$

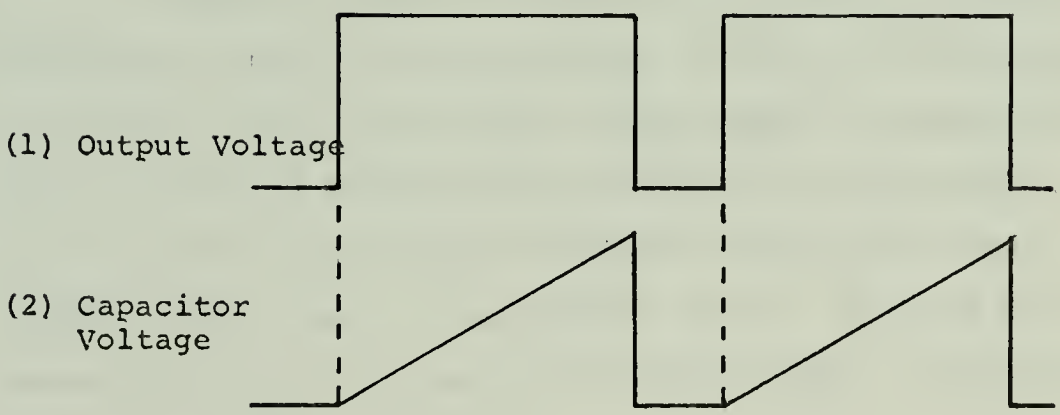
a. Linear-Ramp Time Interval for 555 Timer

The time interval for the 555 Timer configured as a monostable multivibrator with a constant current source charging the external capacitor (see figure 38) is derived as follows:

Knowing $Vc=\frac{1}{C}\int Idt$ where I=Ic, $Vc=\frac{2}{3}Vcc$, dt=Δt,



(a)



(b)

Figure 38. (a) Linear Ramp Configuration, (b) Related Waveforms

and solving for pulse width

$$\Delta t = \frac{\frac{2}{3}Vcc(C)}{Ic}$$

Next assume that $Ic \simeq Ie$ and $I_1 \simeq \frac{Vcc}{R_1+R_2}$

$$Vcc = ReIe+Vbe+(\frac{Vcc}{R_1+R_2})R_2$$

Solving for emitter current:

$$Ie = \frac{R_1Vcc-(R_1+R_2)Vbe}{Re(R_1+R_2)}$$

finally

$$\Delta t = \frac{\frac{2}{3}Vcc(Re)(R_1+R_2)C}{R_1Vcc-(R_1+R_2)Vcc}$$

b. Derivation of Pulse Widths for Digital/Linear Encoder with Constant Current Sink

Figure 39 shows an equivalent circuit for the charge/discharge portion of this encoder. Switch S1 closes whenever Vc exceeds 2/3Vcc and remains closed until Vc equals 1/3Vcc. Switch S2 closes whenever the capacitor is discharging. Figure 40 gives the capacitor waveforms and related times. The problem is to find T as a function of Re. The time Tr is known to be .693RaC from the 555 Timer product information. To find Td begin as follows:

$$I = C\frac{dV}{dT} \qquad (1)$$

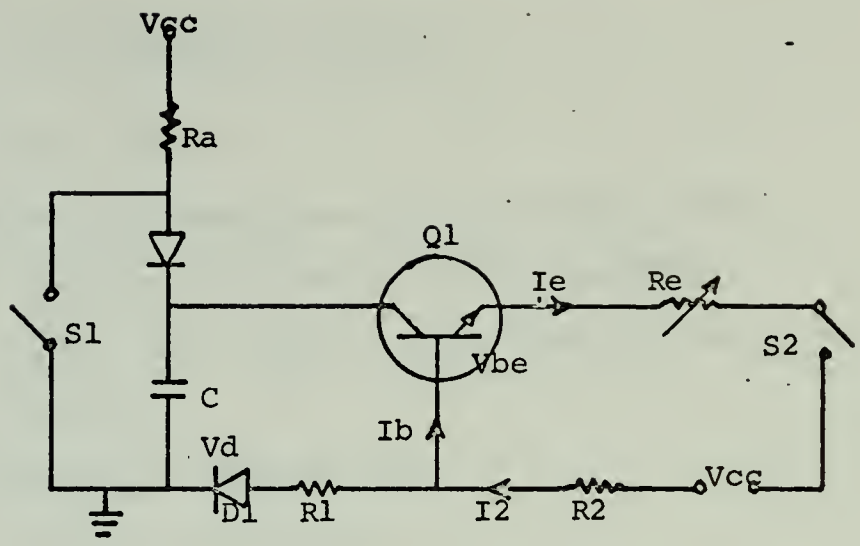


Figure 39. Equivalent Circuit for Constant Current Sink.

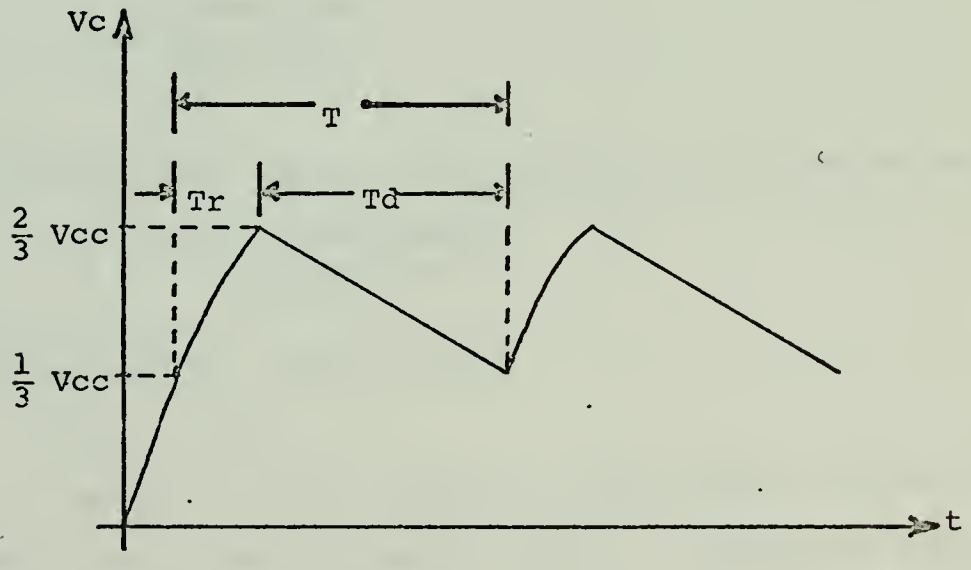
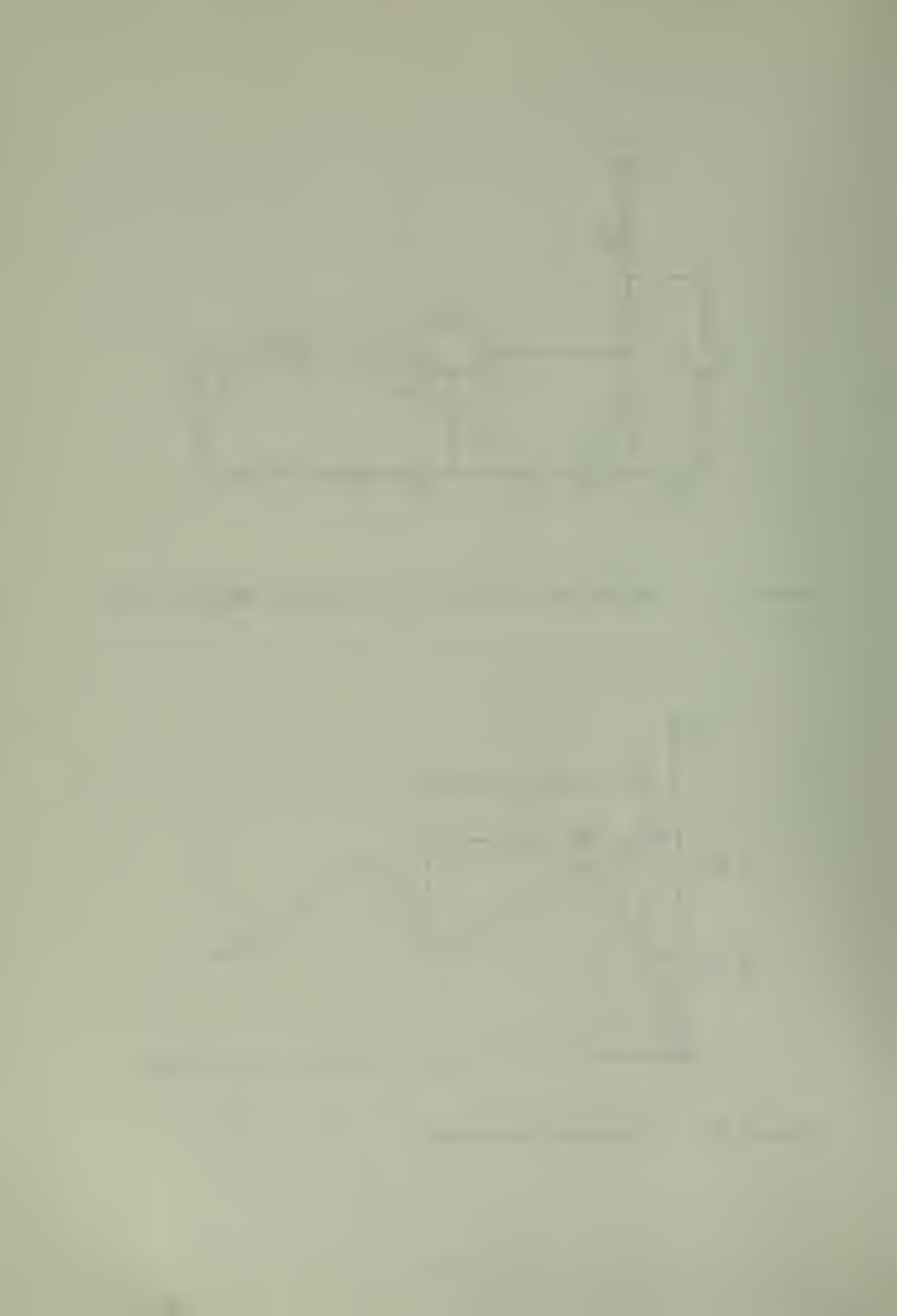


Figure 40. Capacitor Waveforms



Where:

$I = Ic \simeq Ie$ assuming transistor's $\alpha \simeq 1$

$$dV = \frac{2}{3}Vcc - \frac{1}{3}Vcc = \frac{1}{3}Vcc$$

$$dT = Td$$

The following assumptions have also been made:

$Vd = Vbe = .3$ (Q1 and D1 are Germanium)

$Vce = 0$ for 74145 internal transistors

$Ib << I2$

Using Kirchoff's Voltage Law:

$$IeRe = Vcc - I_2R_2 - Vbe$$

Where:

$$I_2 = \frac{Vcc - Vd}{R_1 + R_2}$$

Solving for Ie:

$$Ie = \frac{R_1Vcc - R_1Vbe}{Re(R_1 + R_2)}$$

Substituting this result into equation (1) Td can be obtained:

$$Td = \frac{(1/3Vcc)Re(R_1 + R_2)C}{R_1(Vcc - .3)}$$

The total channel time is then:

$$T = Tr + Td$$

Table VII below lists the comparisons of actual observed output times and output times as calculated above. Column 1 shows the variation in potentiometric positions (simulating sensor outputs, column two and three list the

outputs from channel three and eight as viewed on a Tektronic Type 422 Oscilloscope, column four lists the output times as computed from the equation obtained from curve fitting (T=.318+.2324Re), and column five gives the theoretical pulse widths.

Rs(KΩ)	T_2(ms)	T_3(ms)	Computed Time(ms)	Derived Time(ms)
2.00	0.80	0.80	0.78	0.77
2.50	0.90	0.90	0.90	0.91
3.00	1.00	1.00	1.02	1.05
3.50	1.15	1.10	1.13	1.21
4.00	1.25	1.25	1.25	1.33
4.50	1.38	1.38	1.36	1.47
5.00	1.45	1.50	1.48	1.61
5.50	1.60	1.60	1.60	1.76
6.00	1.70	1.70	1.71	1.90
6.50	1.80	1.82	1.83	2.04
7.00	1.95	1.95	1.95	2.18

Table VII. Comparison of Theoretical and Observed Pulse Times

3. DECODER CALCULATIONS

Assuming that the time multiplexed encoder output contains a 3ms (or greater) sync pause, the pulse width (t_q) of the 9601 can be set to 2.5ms. This will ensure that no channel is long enough to allow relaxation of the 9601 except the sync pause. The 9601 quasi-stable output time is given by:

$$t_q = 0.36RsCs$$

Letting t_q = 2.5ms and choosing a practical value for C (0.1μF), Rs can be found:

$$Rs = \frac{2.5\times10^{-3}}{(.36)(.1\times10^{-6})} = 69.4k\Omega$$

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This paper describes the design and testing of a miniature multi-channel digital telemetry system designed specifically for use in remote controlled model aircraft experiments coordinated by the Aeronautical Engineering Department at the Naval Postgraduate School. The avionics package comprised of data encoder/multiplexer circuitry and a transmitter is lightweight, inexpensive, small in physical size, has low current

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Block 20 - ABSTRACT (Cont)

drain and is capable of transmitting up to nine channels of data. The system was designed specifically for transducers with potentiometric outputs although transducers having voltage or current outputs can be interfaced with the system.

The thesis emphasizes the engineering design requirements and working design models to achieve efficient system performance.

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